

Verification of Singulated HBM2 stacks with Die Level Handler, and review of Wafer Level Sort Challenges

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Agenda

1. *Aggressive Adoption of HBM Memory*
2. *HBM process flow and test insertion review*
3. *Singulated Stack Direct micro-bump probing challenges*
4. *Sacrificial DFT pad probing challenges*
5. *Future work*

HBM Adoption Rate- More Bandwidth Hungry Applications

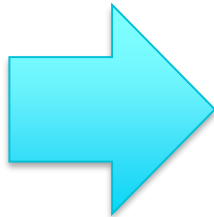
Strong Market Demand for High Bandwidth Memory – Just the beginning!

2.5D/3D advanced packaging enabled a new generation products/solutions for graphic, AI, and deep learning – AMD, NVIDIA, Intel, Google, NEC, Fujitsu

- Recent report from “ResearchAndMarket” with bold forecast for HBM & HMC
 - \$1B in 2018 with path to \$3.8B by 2023, a 33% CAGR
- Applications expanding beyond Graphic into AI, Servers, and Supercomputer



Tesla P100



Tensorflow Accelerator

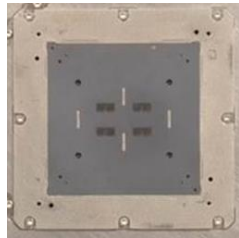
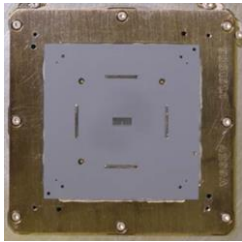


AI Accelerators with integrated HBM

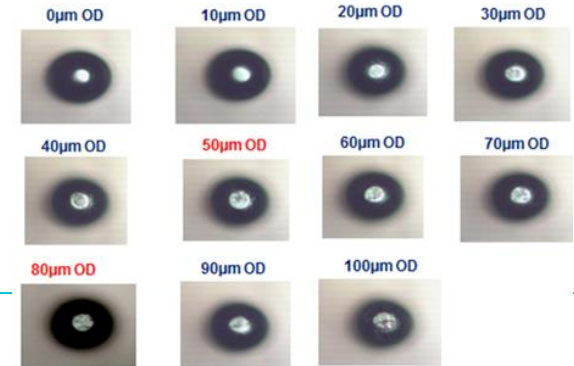
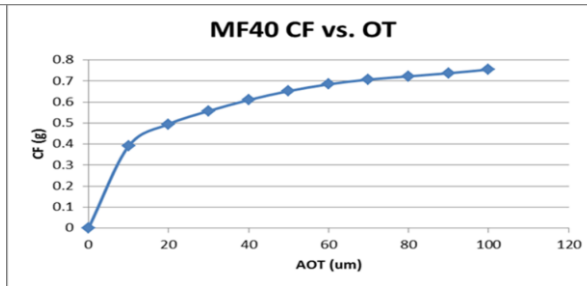
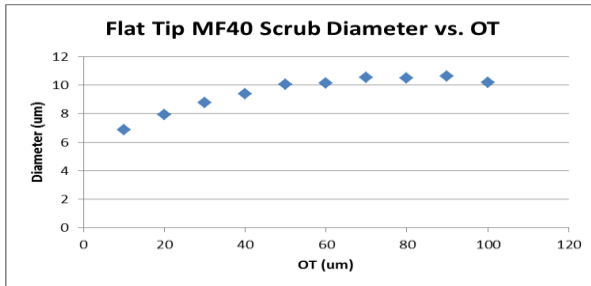
- Google Tensorflow
- NVIDIA Tesla
- Intel Nervana
- Intel Stratix 10
- Xilinx Virtex UltraScale
- NEC Supercomputer
- Baidu

Direct Micro-bump- probing challenges

- **X1 and X4 Configuration** → ~5,000 and ~10,000 probes
- **Bump indentation d/D**
- **Low K MEMS spring** – CRES achieved with minimum K
- **Spring K designed to minimize bump damage across OT range**



Main Specification	Capability
Probe technology	Vertical MEMS/Flat Tip
Probe tip material	PM4 – FFI proprietary
Tip dimension	22 x 24 μm
Probe length from lower GP	2.8mm typical
Maximum allowable OT	80 μm (50-60 μm recommended)
Probe force at recommended OT	0.6-0.8 g
ISMI CCC (Max DC current, 25C)	180mA
Max Allowable Current (MAC)	120mA
Tip XY alignment	+/- 10 μm
Planarity	\leq 25 μm
Test frequency	2 GBps (1 GHz)- validated 3.2GBps (1.6GHz)- in evaluation

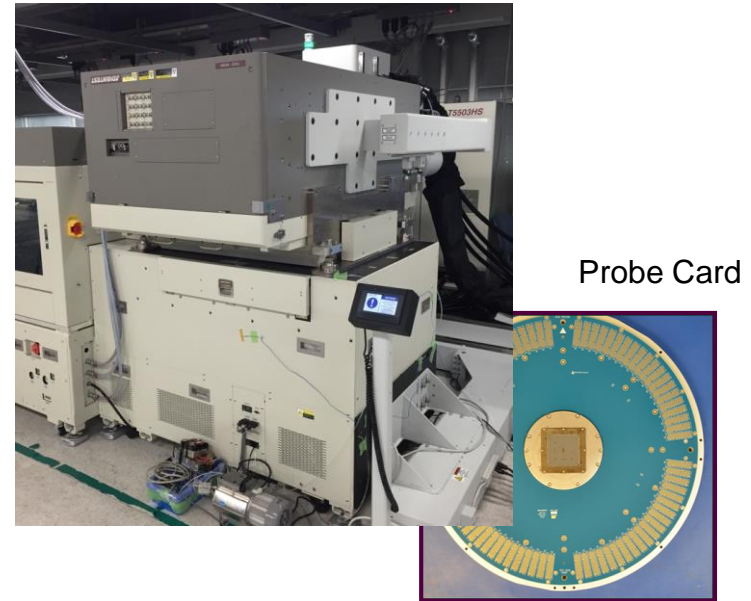
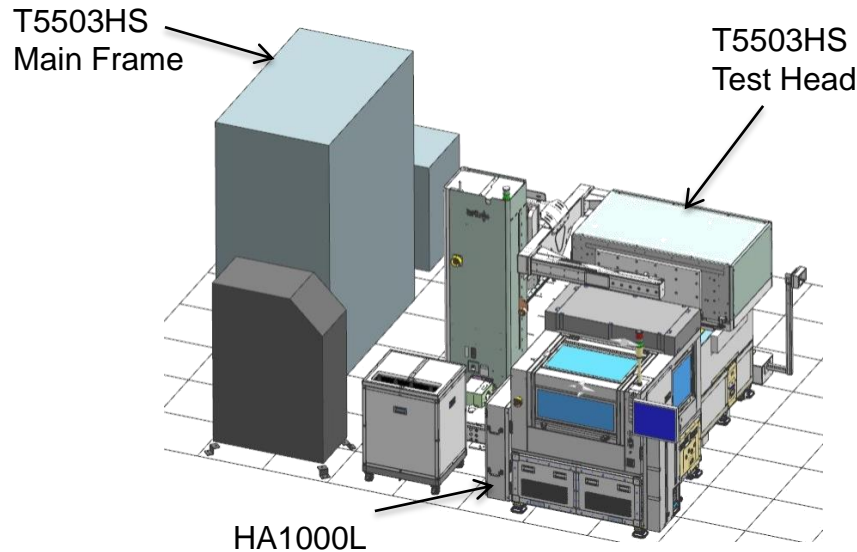


Direct micro-bump probing – Bare Die Handler

Die Handling & Micro Bump Contact are needed

HBM KGSD Test Solution

- HA1000L : Die Level Handler (Advantest)
- T5503HS : Memory Test System (Advantest)
- Probe Card : Probe Card for HBM (FFI)

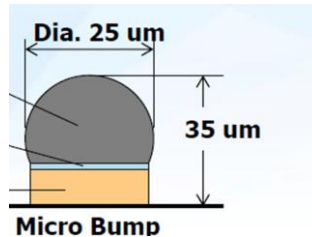


Direct micro-bump probing – HBM2 KGDS Test Result

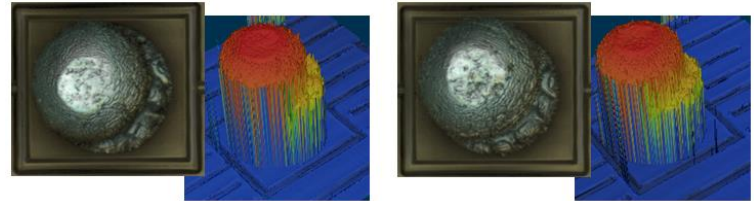
- We succeeded in contacting all I/O pins
- Ambient scrub mark and result
 - Contact Time:6sec, Contact : 1 time vs 2 times
 - Contact Time:600sec, Contact : 1 time vs 2 times

-The scrub becomes deeper as the number of contacts increases
 -The scrub becomes deeper as the test time becomes longer

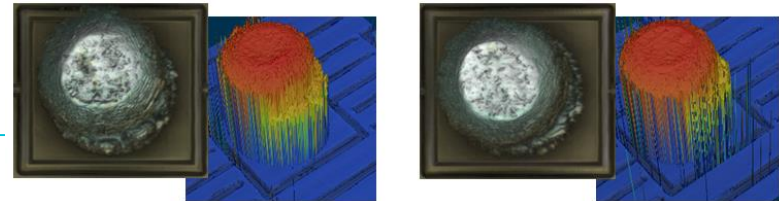
uBump Diameter : 25um
 Over Drive : 60um
 Temperature : Ambient



Condition	T.T:6sec 1 time	T.T:6sec 2 times
Scrub depth[um]	0.87	1.72
Scrub diameter[um]	10.86	10.86

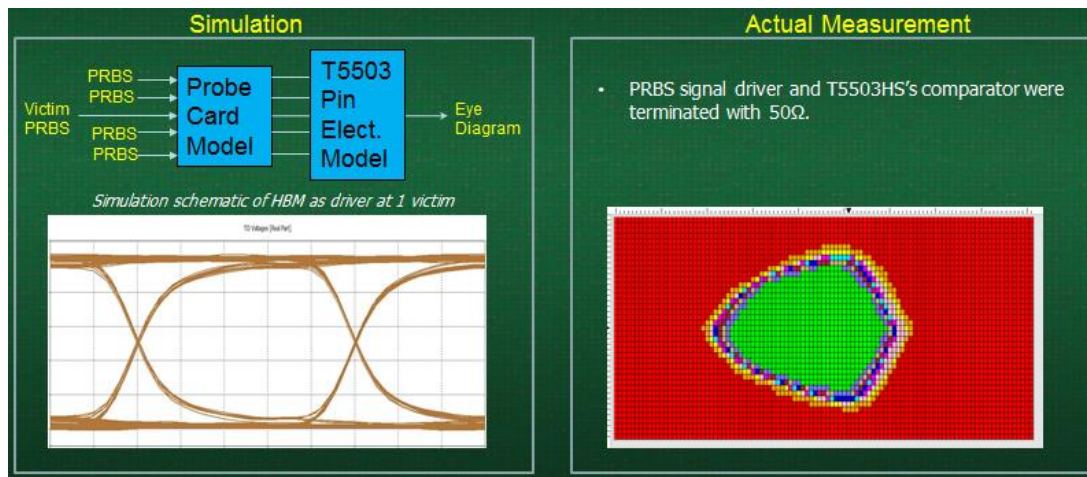


Condition	T.T:600sec 1 time	T.T:600sec 2 times
Scrub depth[um]	2.61	2.99
Scrub diameter[um]	14.81	15.04



Signal Output/Input Performance on HBM2 Die

- **We Simulation vs Actual Measurement result @ 2Gbps**
 - The waveform is similar in simulation and actual measurement on HBM2 die
 - Strong eye-diagram performance correlation



Sacrificial Pad “DFT” - Probing

FormFactor is also a leading probe card supplier for the sacrificial pad probing insertion on HBM pre-singulated wafer and stack wafer–

- FFI SmartMatrix 1500XP and SmartMatrix 2000XP are the main products for probing HBM base die, HBM core die, and final HBM stacked wafer in 4Hi and 8Hi configurations.

“DFT” Pad Probing Challenges of HBM Stack Wafer

Stacking Wafers and The Expected Thermal Induced Challenges of Composite Wafer

Possible Challenges on Composite Wafer

- Wafer Warpage- pad XY coordinate changes
 - Wafer CTE changes vs Silicon wafer
 - Wafer CTE variations between stack configurations
- Basically a “moving target” from the probing perspective

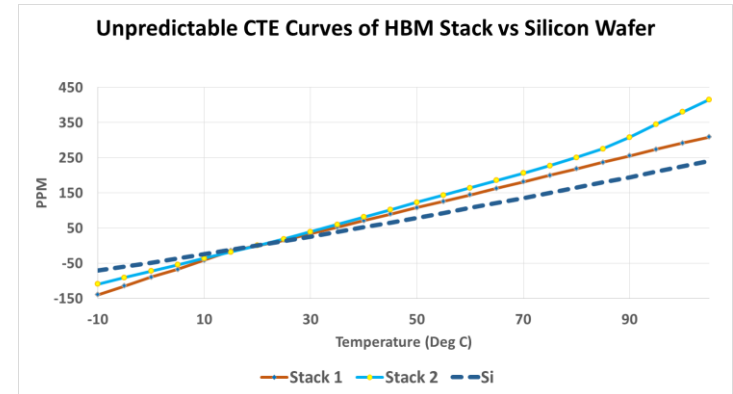
Challenges & Considerations for 3D Packaging
 - Mechanics → Packages only stay flat only in powerpoint!

Die - low CTE (3ppm/K)
 Substrate Higher CTE (14-30ppm/K)
 $T > T_{\text{room}}$
 T_{room}
 Warpage/Flatness

Shape usually flips with temperature ☹️

semiconductors EUROPEAN 3D SUMMIT

Source: SEMI



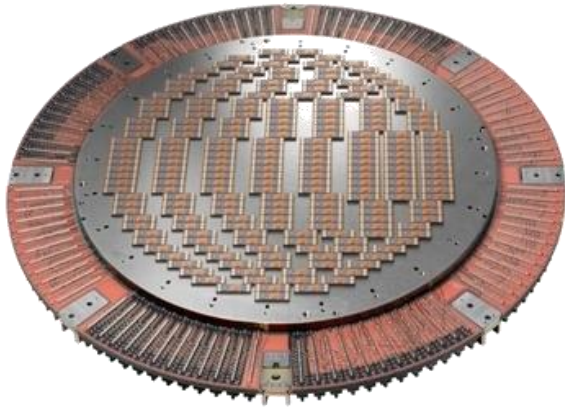
Addressing the “Moving Target” Concern of HBM Stack Wafer

- **SmartMatrix DUTlet based solution for probing HBM stack wafer**



- **DUTlet positioning or placement flexibility**

- *DUTlet XY position scaled to match composite wafer CTE*
- *Automatic pick-and-place for the needed precise accuracy*
- *Like the individual spring/probe, the DUTlets are individually replaceable for best manufacturing yield*



- **The wafer side stiffener (WSS) substrate material flexibility**

- *DUTlet are attached to a WSS metal substrate*
- *WSS substrate advantage – the ability to select desired material with CTE that matches the various composite wafer configuration*
- *Enables probe card to precisely tracks wafer expansion at hot and cold temperature*
- *Single temperature and Dual temperature operation*

Thank You!

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