COMPASS

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FormFactor™

Hybrid MEMS Probe Technology for Advanced Mobile and High-Performance Computing Applications

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Overview

- In this paper, we will discuss FFI's solution to address the challenges of probing advanced technology node processors


BACK IN MY DAY
ONE SIZE FIT ALL
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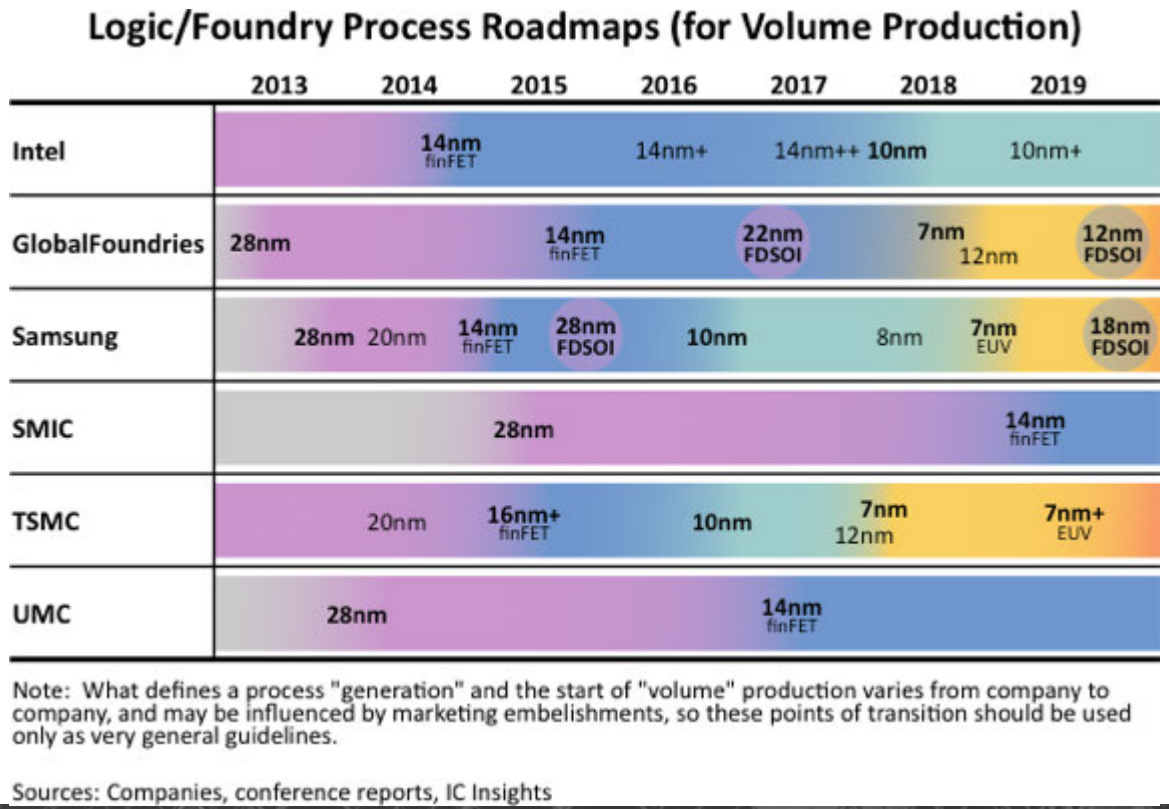
ONE SIZE FITS ALL?
FALSE.
ALL SIZES FIT ONE

Advances in Logic IC Process Technology Move Forward



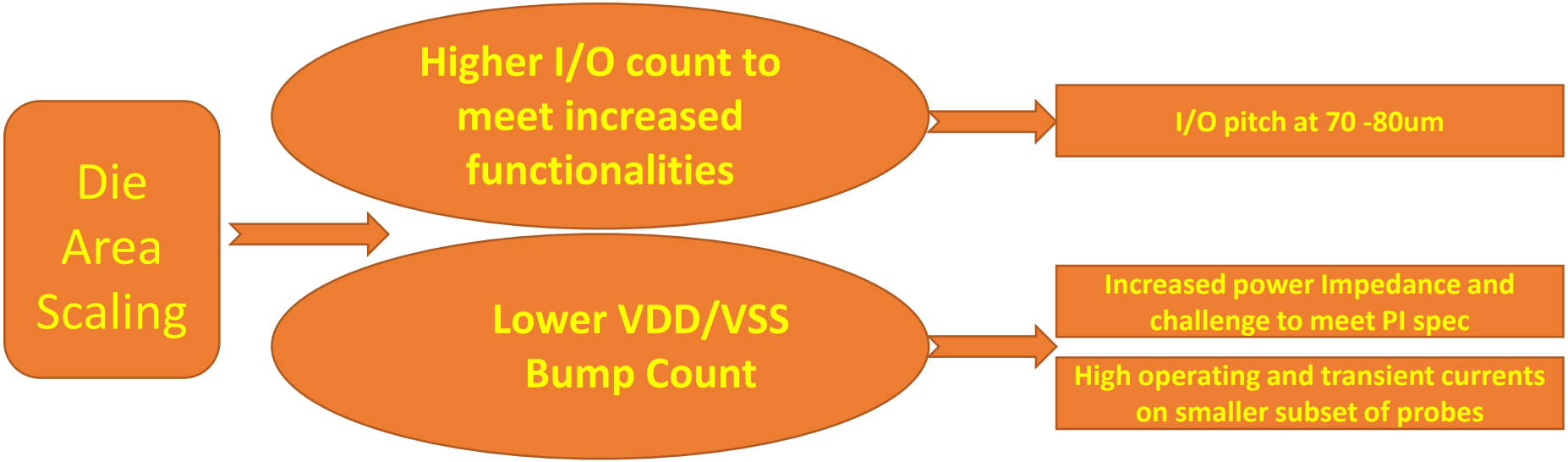
Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embelishments, so these points of transition should be used only as very general guidelines.

Sources: Companies, conference reports, IC Insights

- Mobile and High Performance Computing (HPC) processors continue to lead the process node transition
- 10nm and 7nm process nodes lead the way in 2019

Wafer Test Challenges

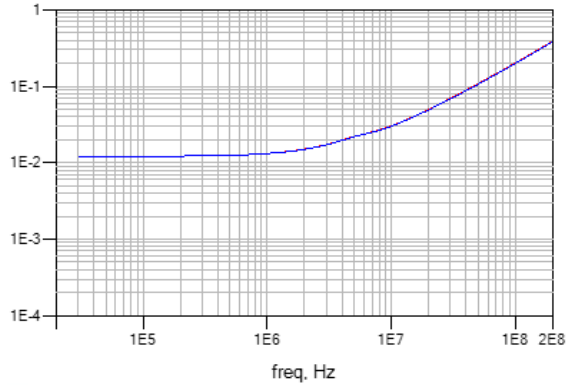
- Leading edge process nodes offer the benefits of smaller die size and lower power consumption
- For wafer test probe cards, this means reduction in probe pitch and power impedance tolerance
- Challenge is to address these two competing requirements with one probe type per design



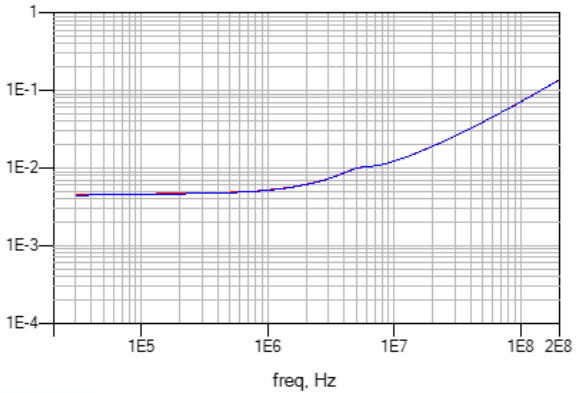
Lower VDD/VSS Bump Count Increases Power Impedance

- Reduction in power bumps and adjacent ground bumps increases power impedance (PI)
  - Due to increase in inductance and reduction in capacitance
- More challenging for probe card design to meet customer PI requirement

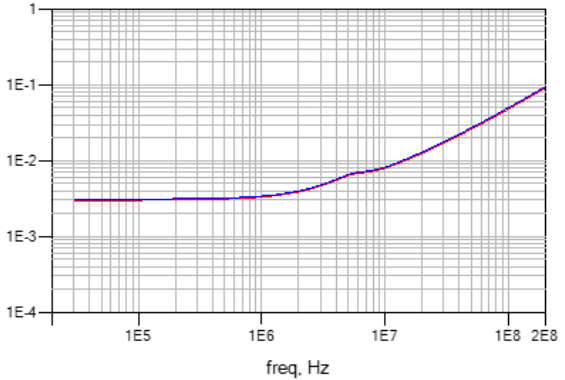
Number of Power Bumps: X



Number of Power Bumps: 2X



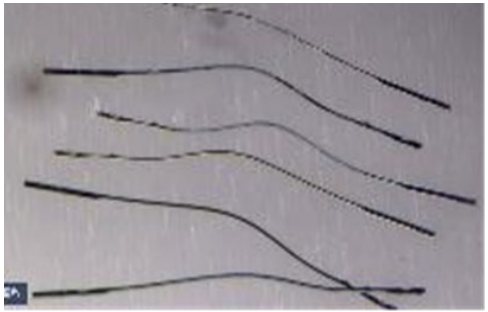
Number of Power Bumps: 4X



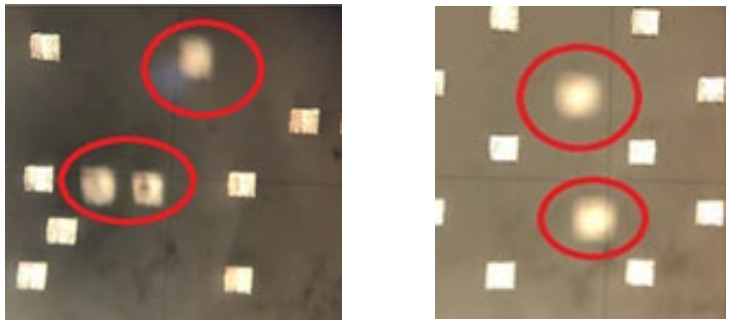
Dynamic Voltage Stress Test Needs Higher Probe MAC

- Dynamic voltage test stresses a device at elevated voltage to eliminate early-life failures
  - Typically at 1.4x to 1.7x device operating voltage
- Devices that fail this test often generate large current surges through a subset of VDD/VSS probes before the initiation of power supply current clamps
- High MAC (Maximum Allowable Current) probe is desired to min burnt probes and max uptime

Deformed Probes due to current exceeding MAC

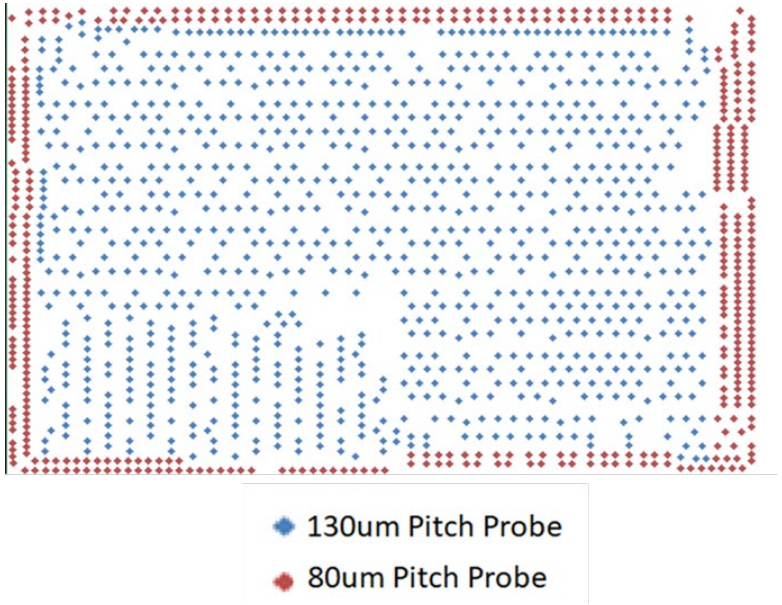


Deformed Probes exhibit planarity change



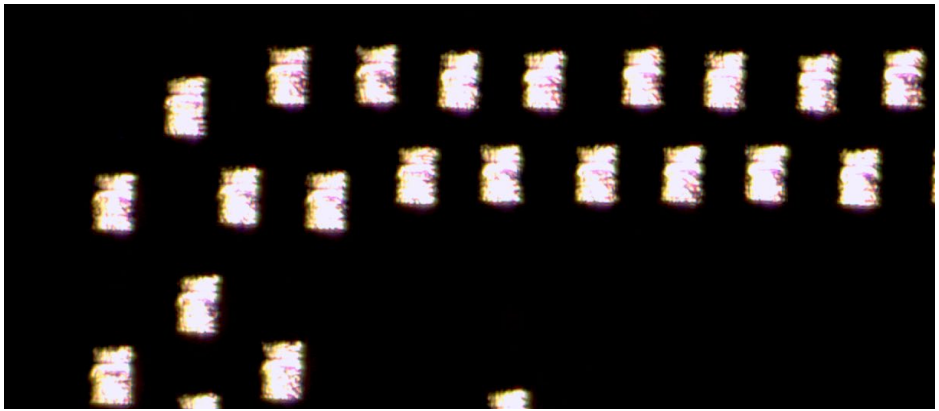
FFI Hybrid MEMS Solution: Fine Pitch, High MAC, Low PI in One Head

- Dual-probe design with composite, multi-material probe structure
- Hybrid MEMS designs use different cross-section probes for different pitches
- Independent optimization of power, ground, and I/O probes
- Use finer pitch probe as needed for IO's on perimeter of the die and larger pitch probes for power/ground bumps for the core area of the chip
- Satisfy multiple requirements, while "de-constraining" from a single-probe design

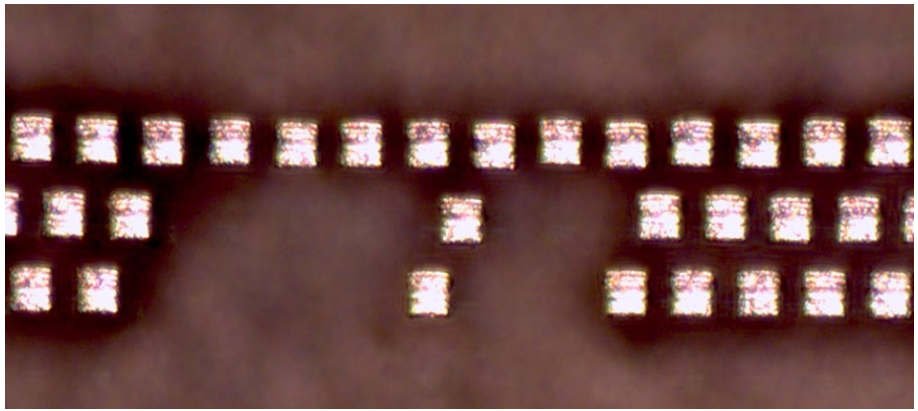


Hybrid (MF80+MF130) offers 60% higher MAC for power probes, resulting in reduction in burned probes

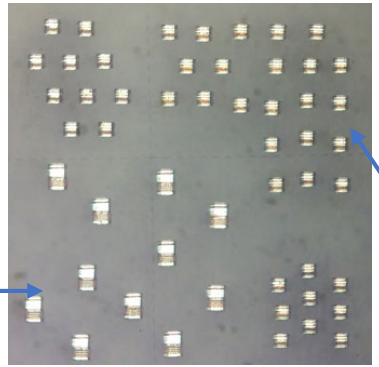
Hybrid MEMS Probe Tips Images



100um Pitch Probe



80um pitch probe

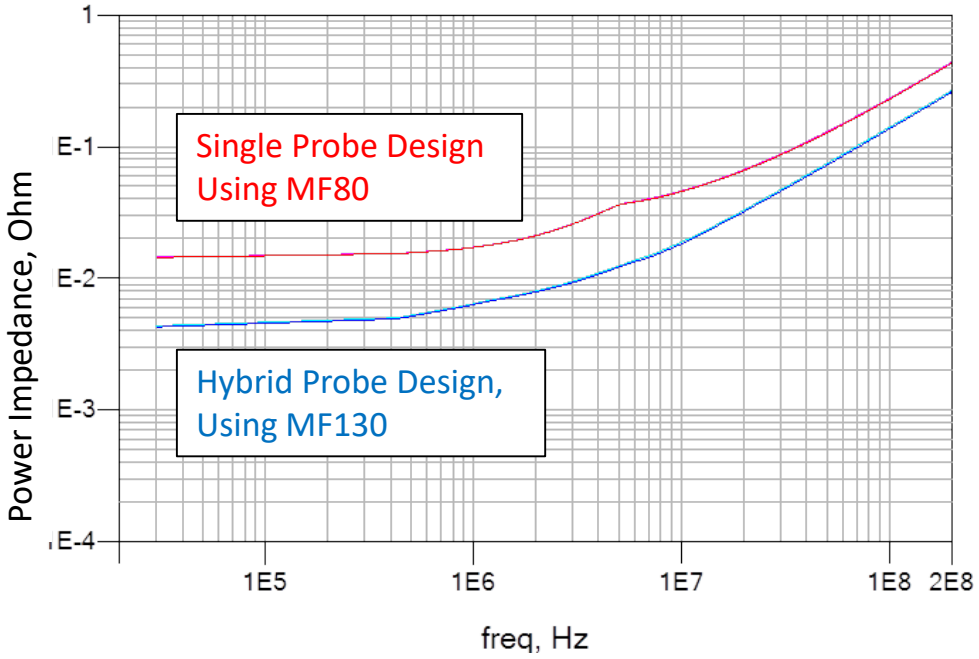


130um pitch probe

80um pitch probe

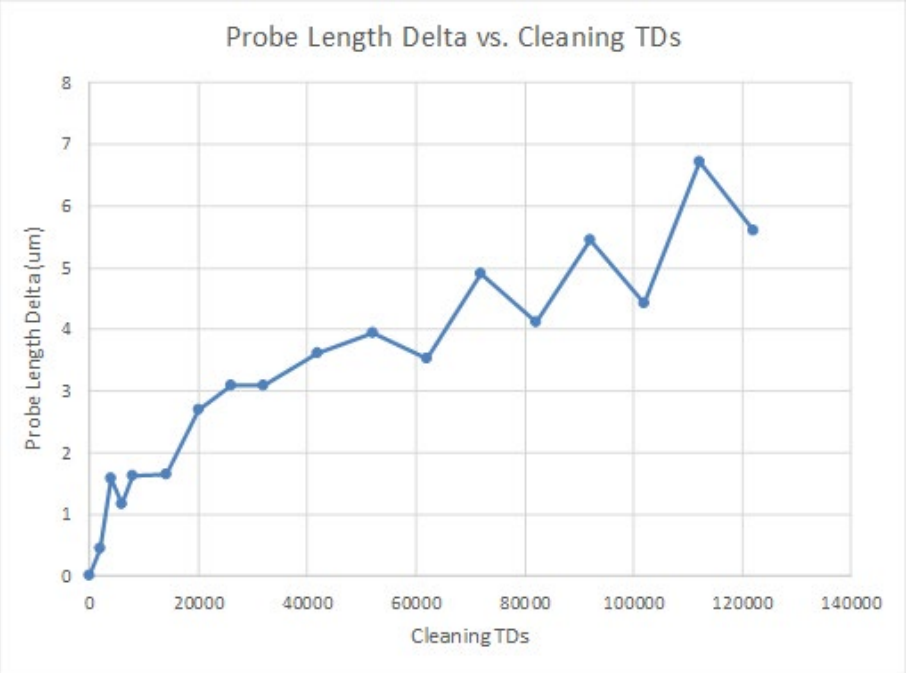
Hybrid MEMS Probe Head Reduces Power Impedance

- PI comparison for critical Power supply with 17 bumps
- PWR & GND (MF130) probes enable
  - 40% lower Power Impedance



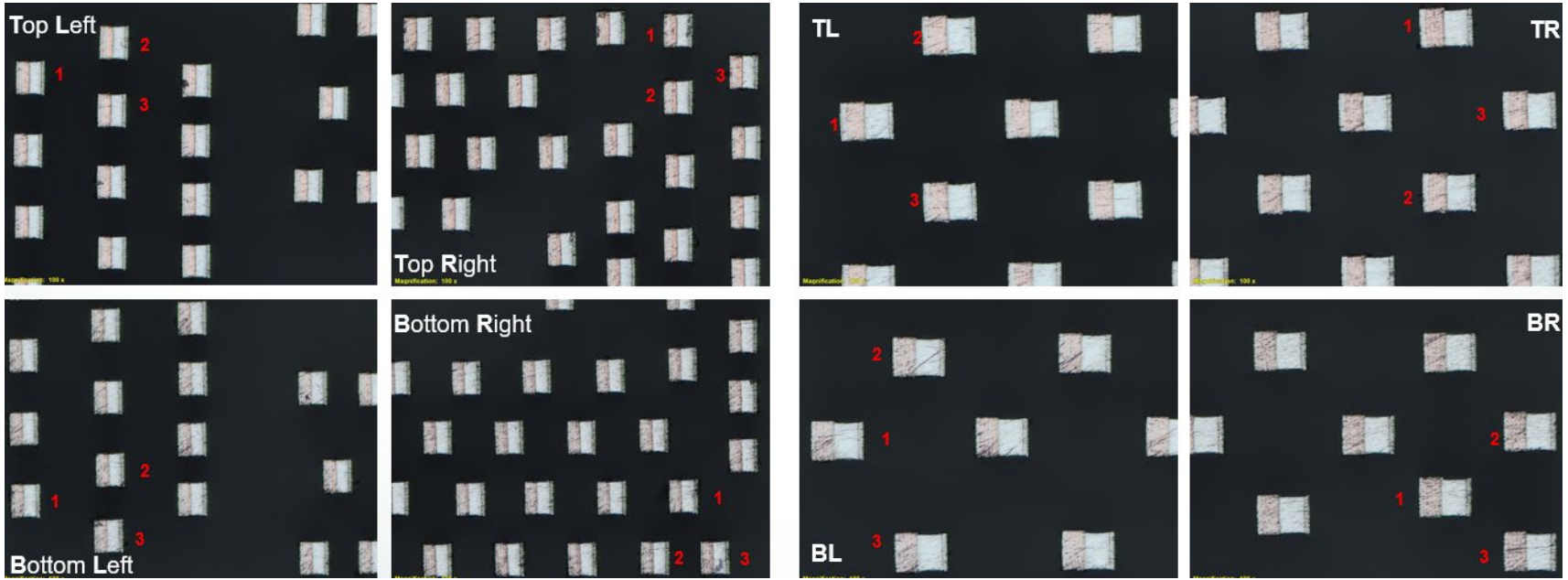
FormFactor Hybrid MEMS Tip Wear Rate Characterization (1/3)

- Wear Rate Experiment Condition
  - Progressive TDs completed on 3M Pink
  - 122k cleaning touchdowns
    - Equivalent of ~1M wafer sort touchdowns
  - 60um cleaning AOT Overtravel
    - Performed AOT/POT test to obtain the POT required to achieve desired AOT
  - Sample probes for each probe type at each corner of array were monitored for wear
- Experiment Results
  - MF130F probes are ~6um longer than the MF80F probes after 1M wafer sort touchdowns
  - This 6um delta is well within acceptable tip length variation within a typical test cell



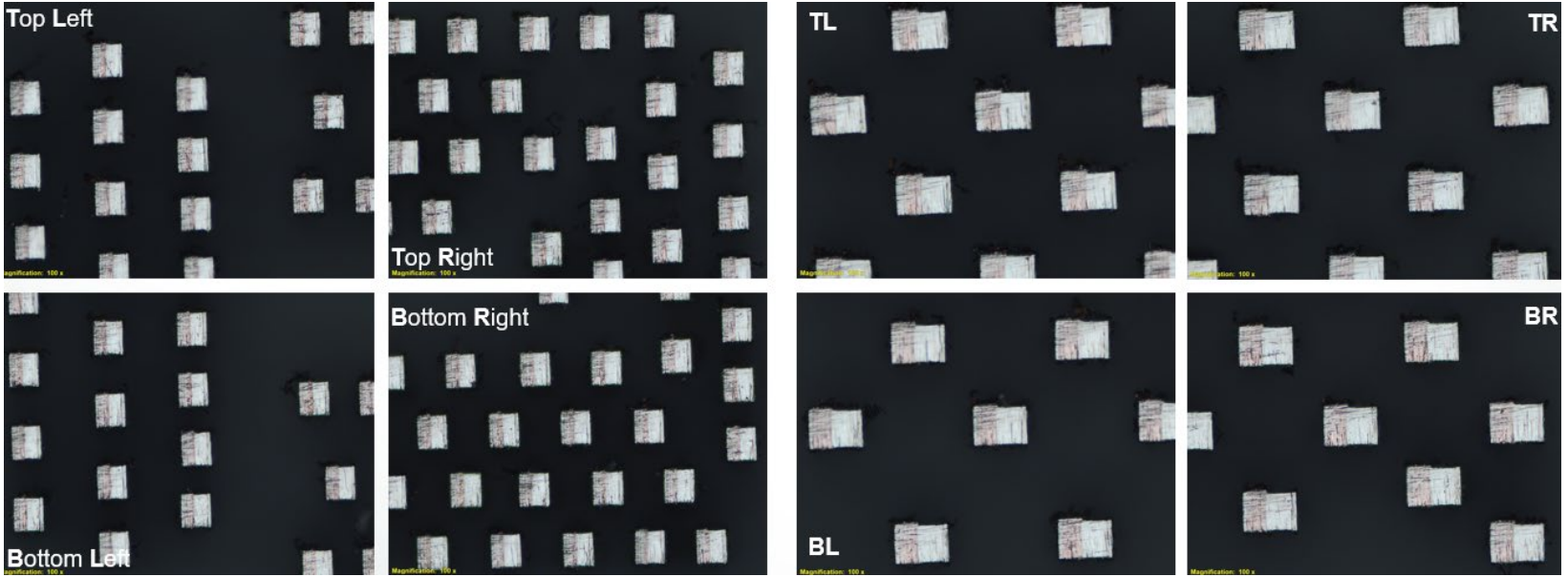
FormFactor Hybrid MEMS Tip Wear Rate Characterization (2/3)

- Hybrid MEMS Probe Card Tip Wear Rate Experiment - Initial Probe Tip Pictures



FormFactor Hybrid MEMS Tip Wear Rate Characterization (3/3)

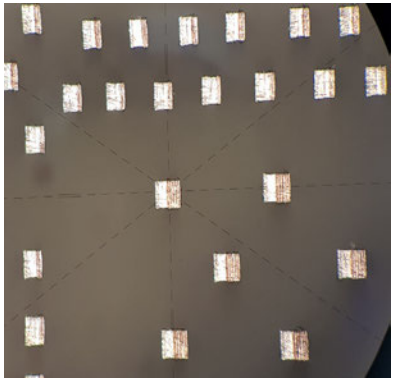
- Hybrid MEMS Probe Card Tip Wear Rate Experiment – Post Wear Probe Tip Pictures



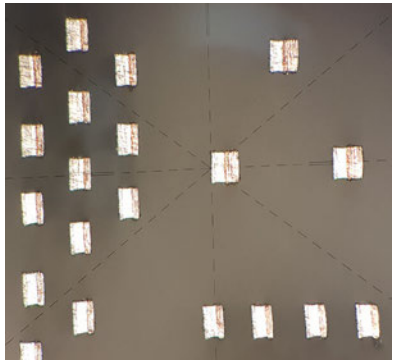
Customer Hybrid MEMS Results: Device X (1/2)

- Design Parameters
  - Total Probes: ~20,000
  - Hybrid Probe Types: ~70% MF100, ~30% MF80
  - Parallelism: 12 (2 x 6 DUT configuration)
  - Bump Material: Cu Pillar
- Results
  - Yield and functional correlation passed with better results than single probe design
  - Expected even tip wear, no noticeable tip length difference after ~26K production touchdowns

Location	MF80-MF100 Delta
Upper Left	1-2
Lower Left	2
Upper Right	2
Lower Right	0
Middle	1


Upper Left


Upper Right

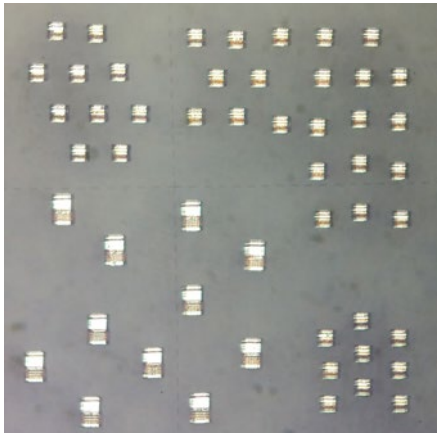

Lower Left

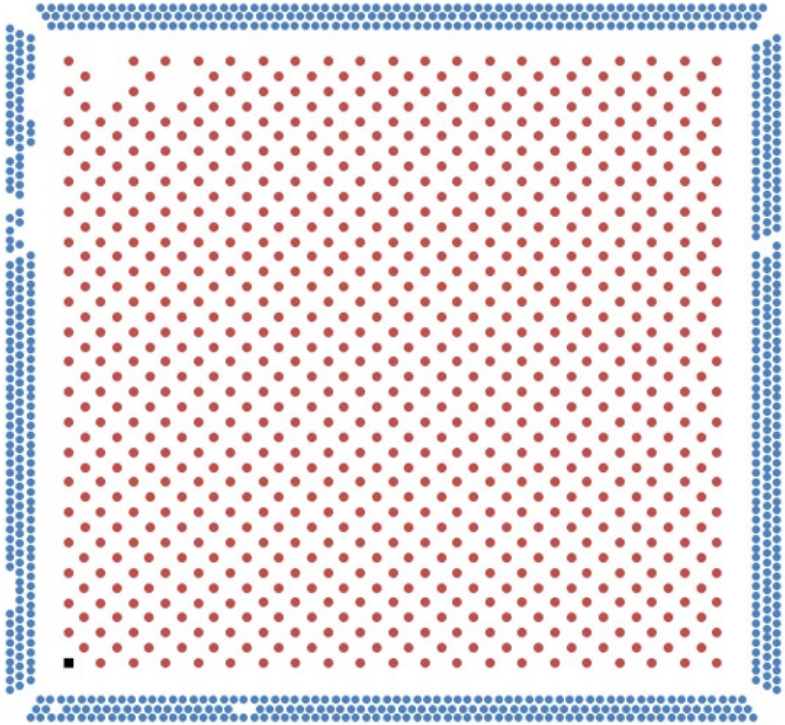

Lower Right

Customer Hybrid MEMS Results: Device X (2/2)

- Design Parameters
  - Total Probes: ~2000 probes
  - Hybrid Probe Type: ~70% MF130, ~30% MF80
  - Minimum Bump Pitch: 80um
  - Bump Material: Cu Pillar
- Results
  - No probe burn events

  MF130F power probes





FormFactor Hybrid MEMS – ALL SIZES FIT ONE

- FormFactor Hybrid MEMS probe technology supports various competing requirements in a single probe head -- fine pitch, high current carrying capability, and lower power impedance
- Composite MEMS probe enables one principal probe design to achieve function/reliability at different pitches – simplify probe qualification process for customer
- Universal performance of hybrid probes has been demonstrated at customer production sites
  - OT, Stress field, assembly, cleaning, maintenance, wear rate