Probe Card Solution to Address Leading-Edge Advanced Package Test Requirements

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Agenda

- **Introduction**
  - Advanced Packaging market and test complexity trend
  - Advanced Packaging key components and test solution overview
- **Probe Card Solution to Address Each Advanced Packaging Component Test Requirements**
  - Matrix HFTAP PC for KGD and HBM KGS test
  - Altius PC for HBM KGSD and Si Interposer test
  - Apollo MEMS PC for SoC CuPillar with solder bump test
  - Kepler MEMS PC for SoC PAD testing
- **Summary and Key Takeaways**

Advanced Packaging Demands More Testing

Advanced Packaging Complexity Trend:

- From simple SoC + HBM to multiple SoC + multiple HBM
- HBM DRAM stack increased
- Package size growing

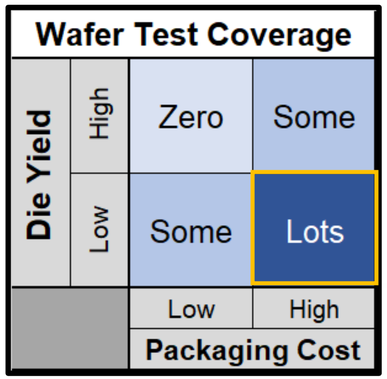
Advanced Packaging Revenue Growth in CAGR 6.6% (2014~2025)

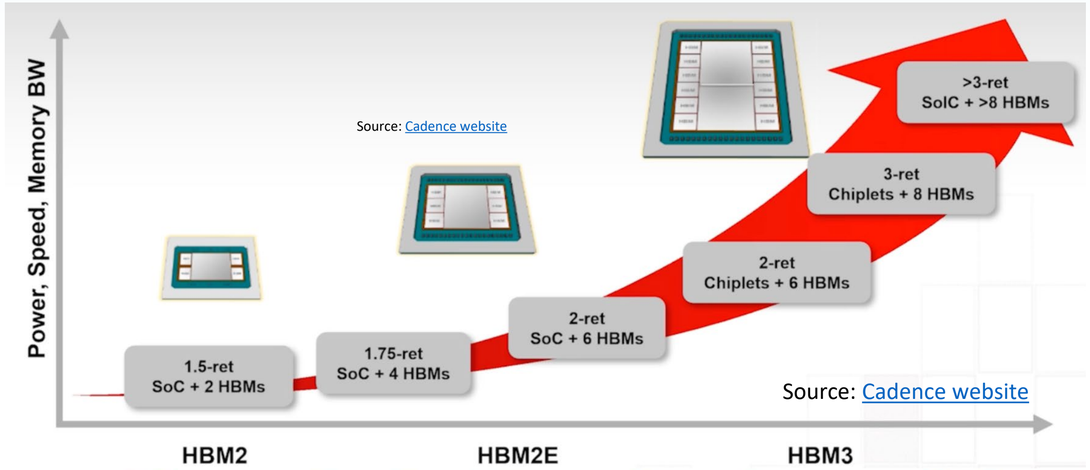
- More chips in the package → high value $
- Advanced Packaging offers more features and computing power than individual IC package results into market growth

Known Good Die/Stack Test Help Reduce Risk and Cost on Advanced Packaging

- Higher complexity → lower yield
- Higher complexity → higher packaging cost
- Earlier defect detection help save packaging cost

https://www.swtest.org/swtw_library/2020proc/pdf/00pm_SWTest_Untethered_Keynote_Slessor_FormFactor.pdf





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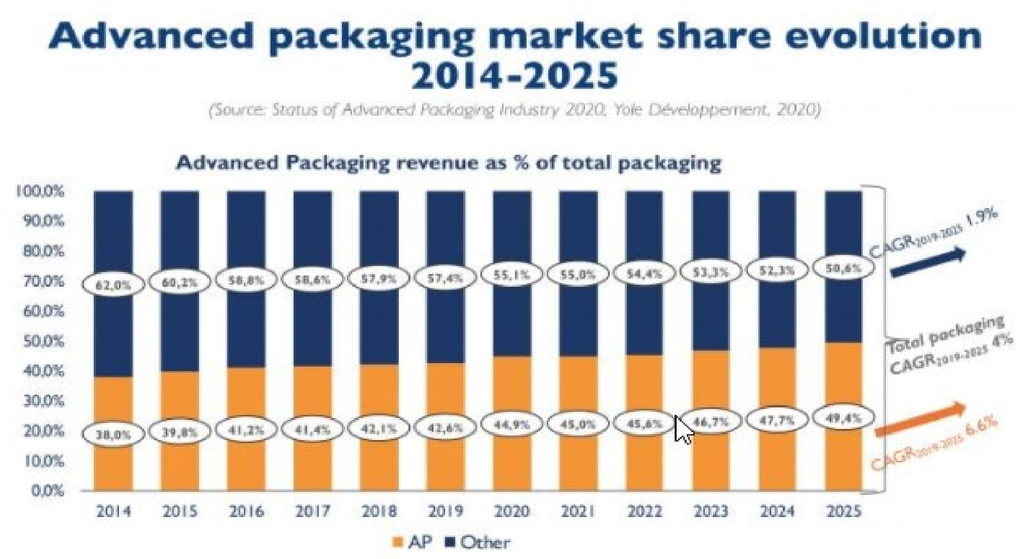
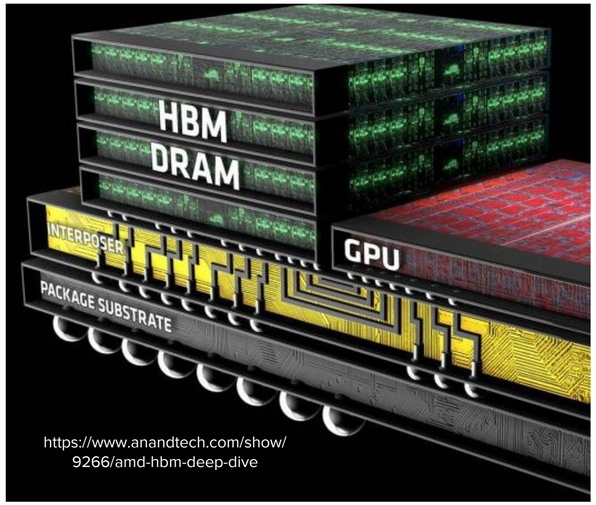
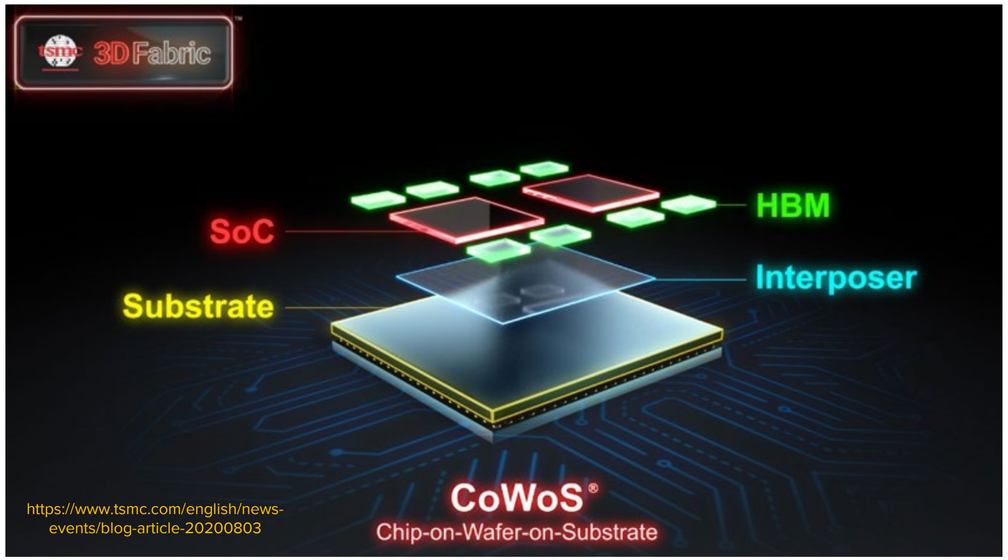


Advanced Packaging Key Components and Its Test Requirements

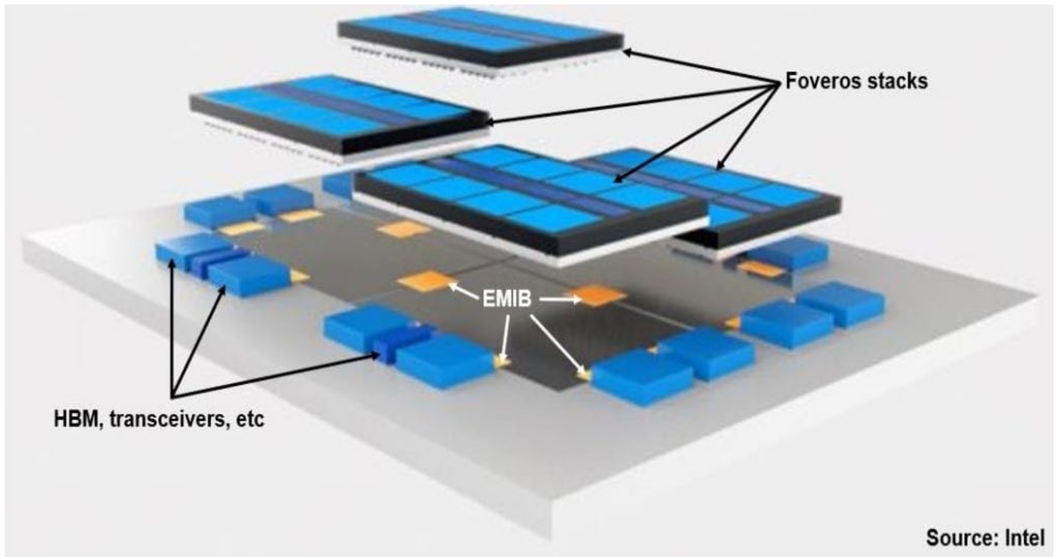
	Test Methods	Key Probe Card Requirements
High Bandwidth Memory	Known Good Die test on DRAM wafer Known Good Stack test on HBM Stack Direct HBM Bump test on HBM Stack Die	High Speed: follows DDRx Spec High Parallelism: 128~256// Fine Pitch: 45um
Silicon Interposer/EMIB	Connectivity Test on HBM/Si Interposer Bump	Fine Pitch: 45um Low Probe Force: <1.5gf
SoC IC	CuPillar Bump Test on SoC Sacrificial Pad Test on SoC	Large Pin Count: 32K ~ 65K Low Probe Force: <3gf Dual Temp Pad Probing



https://www.anandtech.com/show/9266/amd-hbm-deep-dive

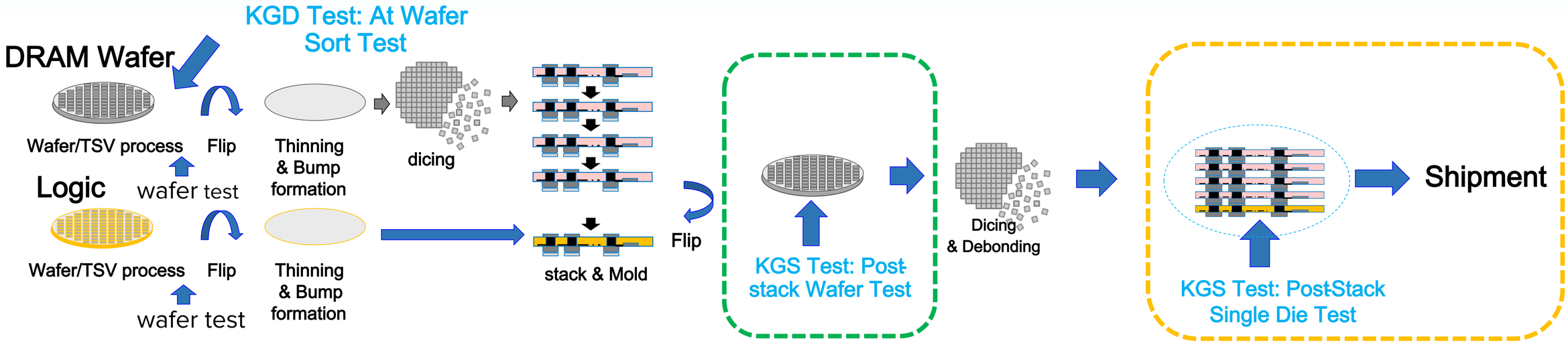


https://www.tsmc.com/english/news-events/blog-article-20200803



https://newsroom.intel.com/news/intel-unveils-new-tools-advanced-chip-packaging-toolbox/#gs.fe8u1i

Choices of Known Good Die/Stack Test in HBM Manufacturing Flow



	Chioce 1 (Known Good Die Test)	**Chioce 2 (Known Good Stack Wafer Test)**	**Chioce 3 (Known Good Stack Single Die Test)**
Where to Test in the HBM Flow	DRAM Wafer Sort	DRAM Wafer Post Stacking	DRAM Stack Die Post Dicing
Probing Interface	Pad on DRAM Die	Sacrifical PAD in HBM Bump Array	HBM Micro-Bumps
Probe Card Technology	DRAM HFTAP Probe Card	DRAM HFTAP Probe Card	Vertical MEMS Probe Card
Advantage	Probing recipe and probe card technology similar to wafer sort test. Earliest detection in HBM Mfg flow	Known good stack result Relatively cost effective solution (high test efficiency and good enough coverage)	Full test coverage, truly known good stack
Challenges	Known good die only, not able to detect defects during wafer stack	Test strategy and DFT build to die design to get good enough coverage Probing recipe optimization for wafer stack and CTE management on composition material	HBM2 bump pitch and signal count challenge space transformer fan out (high cost) Probing recipe develop on single die stack handling

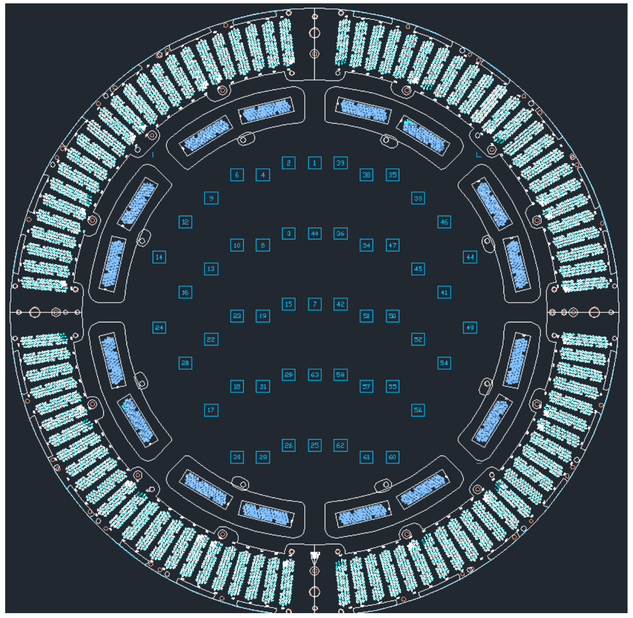
Probe Card Solutions Case Study: KDS HBM2 and KGD LPDDR4

KGS HBM2 Probe Card

Max 64DUTs, 18TD, T11.2P (-40~150°C)

Target Speed 3.2GHz

Advantest T5503 HS2 H7-010508

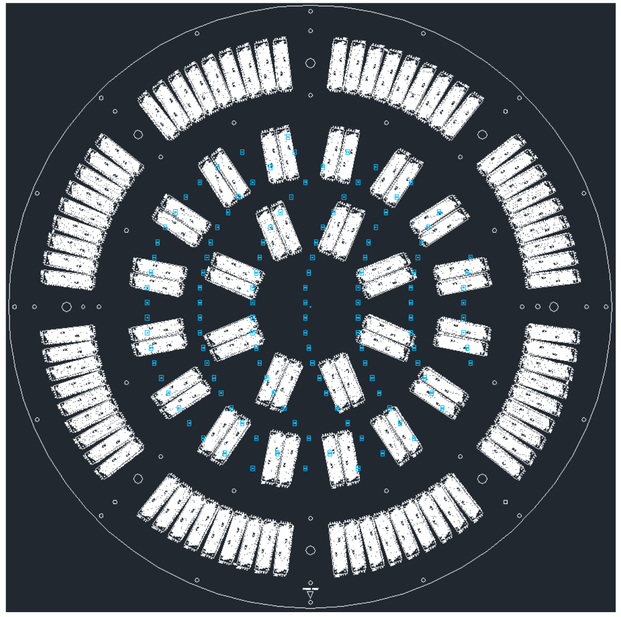


KGD LPDDR4 Probe Card

Max 128DUTs, 45TD, T11.2P (-40~150°C)

Target Speed 3.2GHz

Advantest T5503 HS2 H7-010569

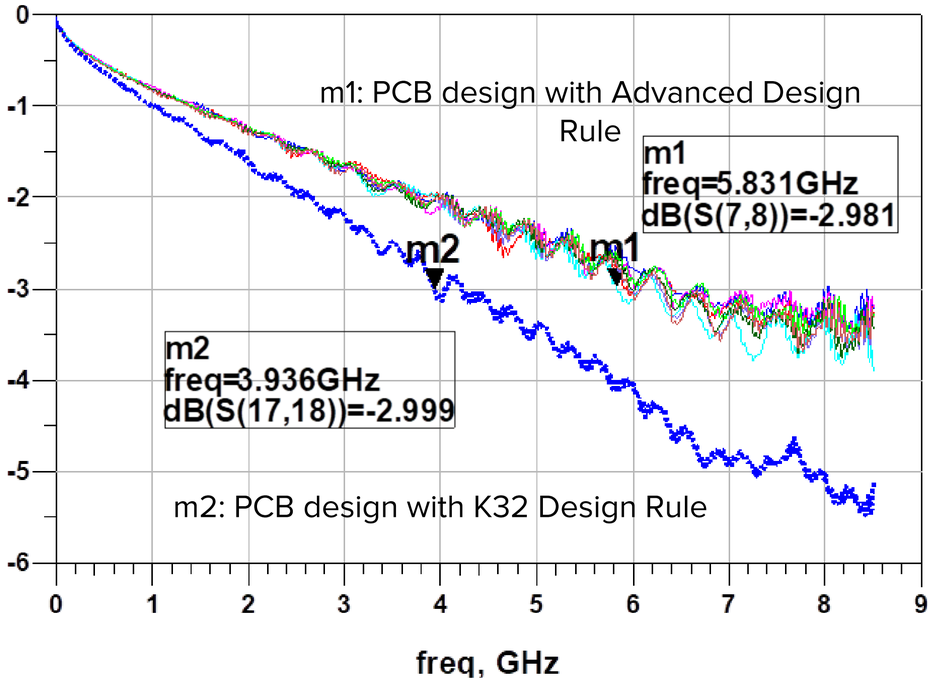


Both Probe Card Solutions Achieve Highest DUT Parallelism and Speed Requirement (>3GHz), T11.2P Offers Wide Temperature Range

Further Improve Probe Card Speed Performance Beyond 4GHz

FFI PCB Design Measurement Result Shows There is Path for Probe Card Support >5GHz KGSD Test Requirement

- Multiple signal channel PCB only simulation
- With advanced design rule (for HFTAP K40 and K50 product)
- Existing tester configuration
- With PCB high speed material and manufacturing rule
- -3dB bandwidth improve by 1.9Ghz

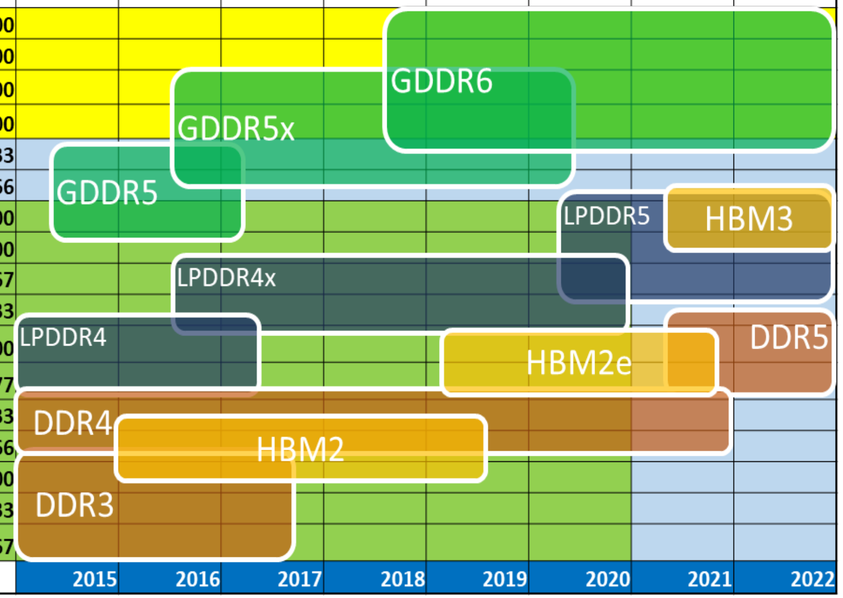


FFI is meeting high speed test requirements, up to 4GHz

- K32 (3.2GHz) is released and running in HVM
- Probe Card architecture proven for >5.0GHz speed
- >4.0GHz development pending ATE roadmap

Memory KGDS Speed Test Requirement vs. FFI Product Line

FFI Product Platform	FFI HFTAP Product Class	Clock (MHz)	Data Rate (Mbps)
		8000	16000
		7000	14000
		6400	12800
		5600	11200
Matrix	K40	4267	8533
		3733	7466
Matrix	K32	3200	6400
		2800	5600
Matrix	K22	2134	4267
		1867	3733
Matrix	K16	1600	3200
Matrix	K12	1339	2677
Matrix	K10	1067	2133
		933	1866
Matrix, PH	K8	800	1600
		667	1333
Matrix, PH	K5	534	1067

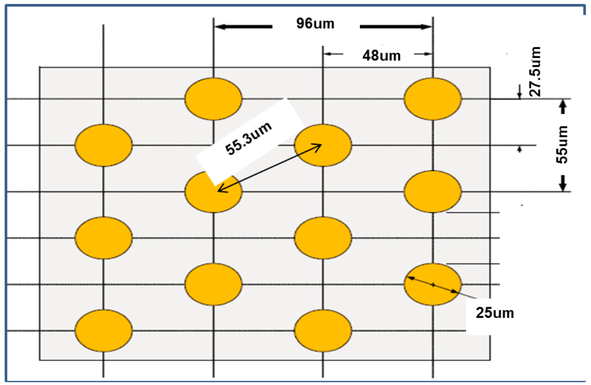


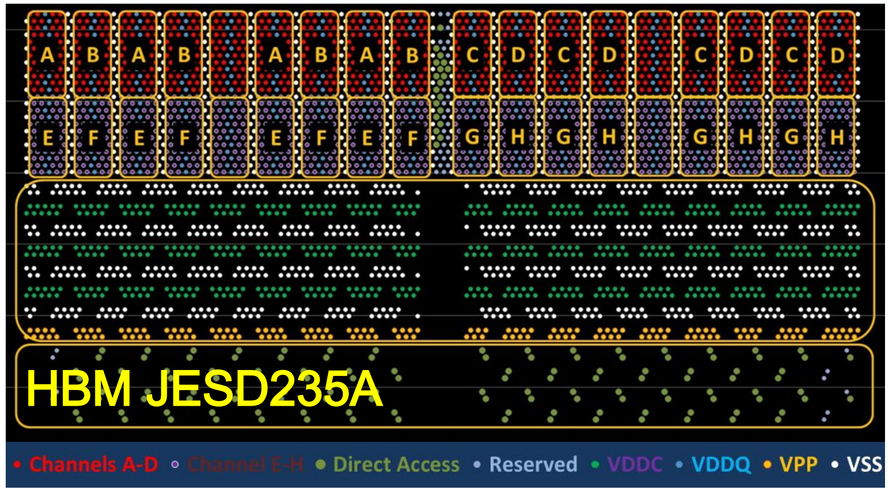
Altius Probe Card for HBM & Si Interposer Testing

Probe Technology

- Sub-50um pitch MEMs Probe (48um x 55um)
- <10um Tip XY Alignment
- Low Probe Force

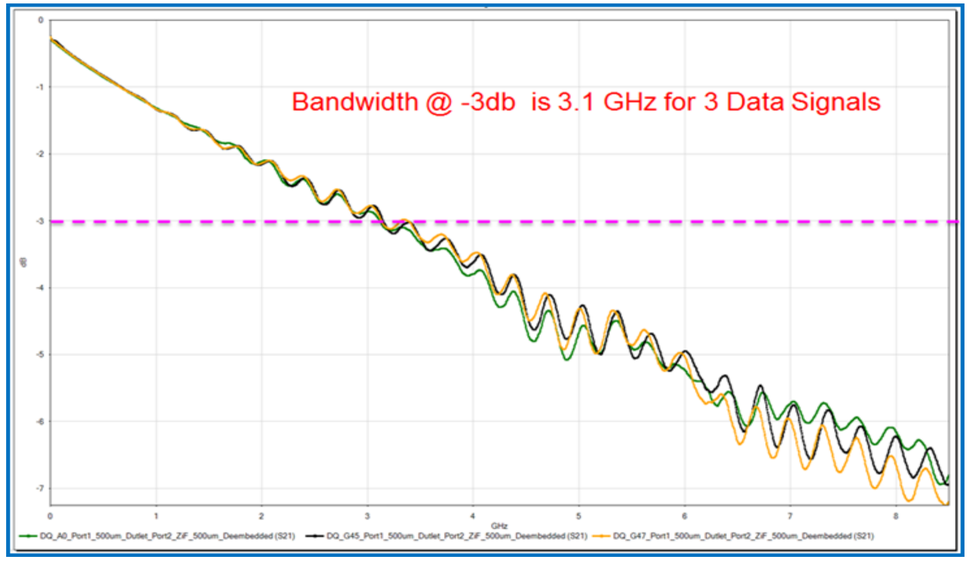
Altius MF45 MEMS Probe





Electrical, Signal & Power Integrity Requirement

- Support at-speed testing > 2.4Gbps
- ~6x3mm die size
- Reliable contact to ~5000 & ~10,000 micro-bumps
- STF design and manufacturing
- Impedance & X-talk optimization
- Maximize performance margin



- Rise time 100pS, 20 to 80%
- 1V swing, no pre-emphasis
- VNA measured data used for eye-diagram simulation @BGA side with 1pF termination

SWTW 2017
SW Test Workshop
Semiconductor Wafer Test Workshop

Verification of Singulated HBM2 stacks with Die Level Handler

Dave Armstrong
Toshiyuki Kiyokawa
Quay Nhin

ADVANTEST
FormFactor Inc.

Altius Probe Card for HBM & Si Interposer Testing

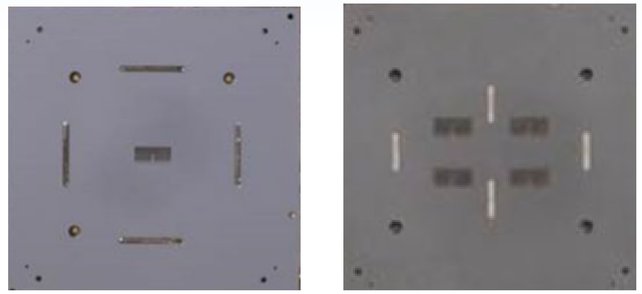
Parallelism

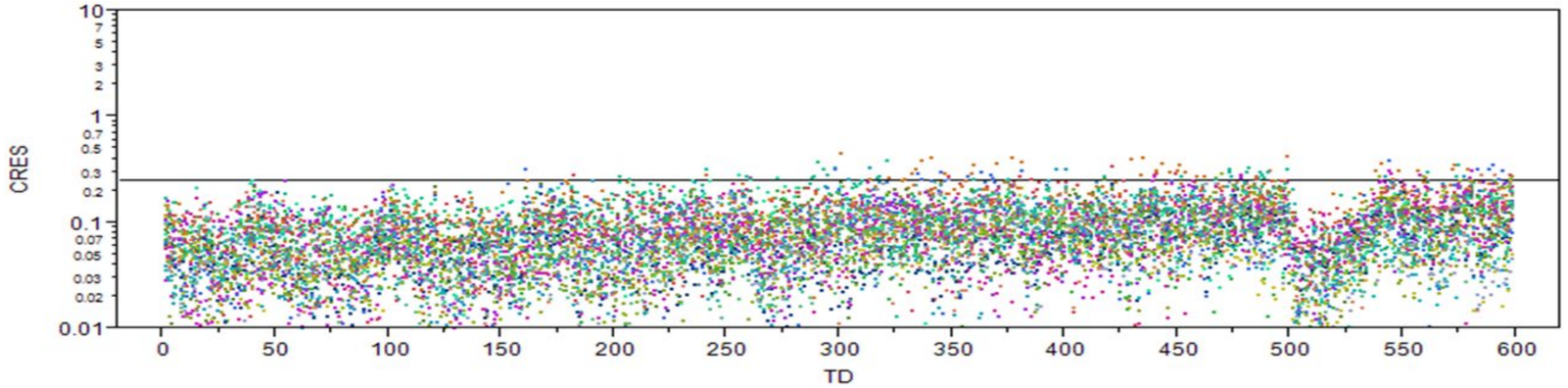
- X1 and X4 Configuration (~3K Probe per Die)

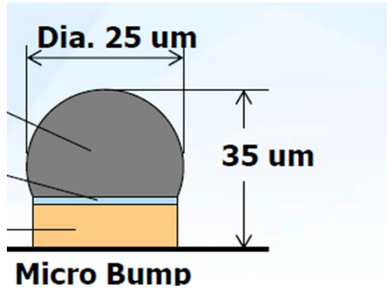
µBump "coining" d/D behavior

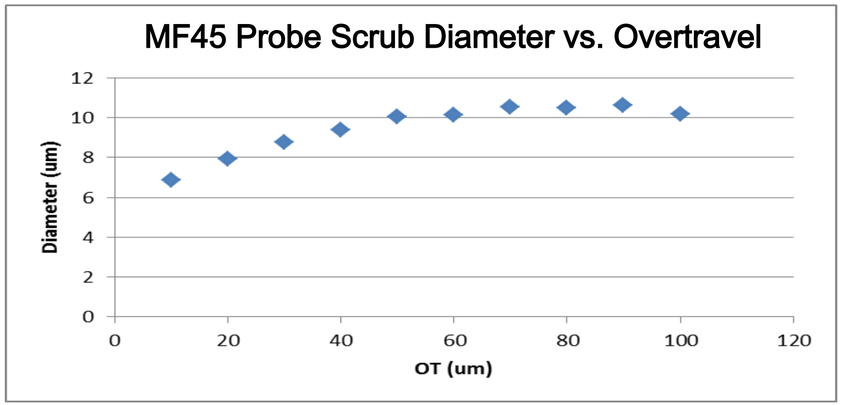
- Probe designed to minimize bump damage across OT range

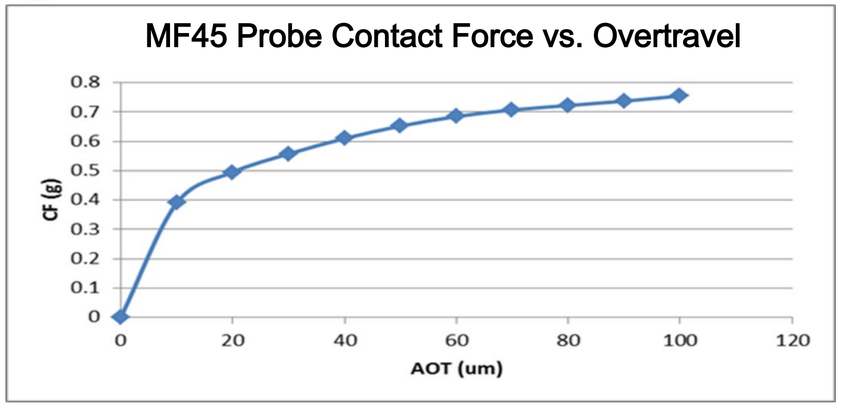
Low Probe Force Stable CRES MEMS Probe– minimum K to achieve good CRES

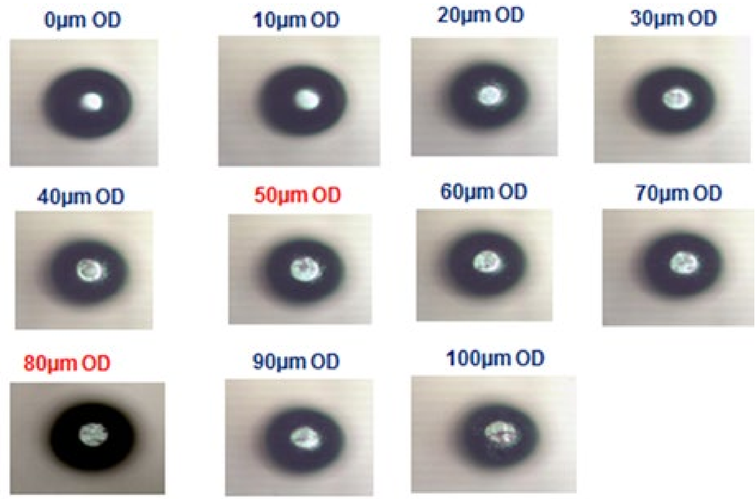






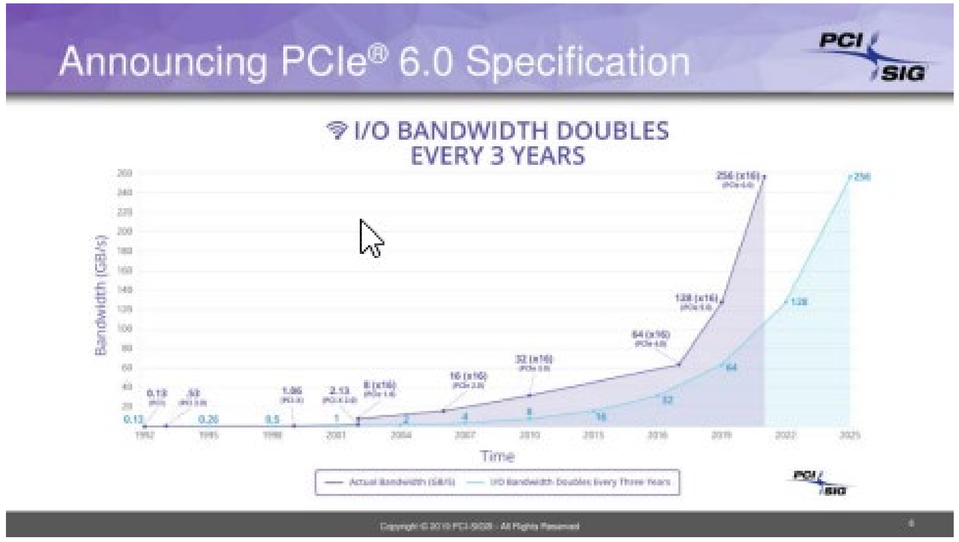


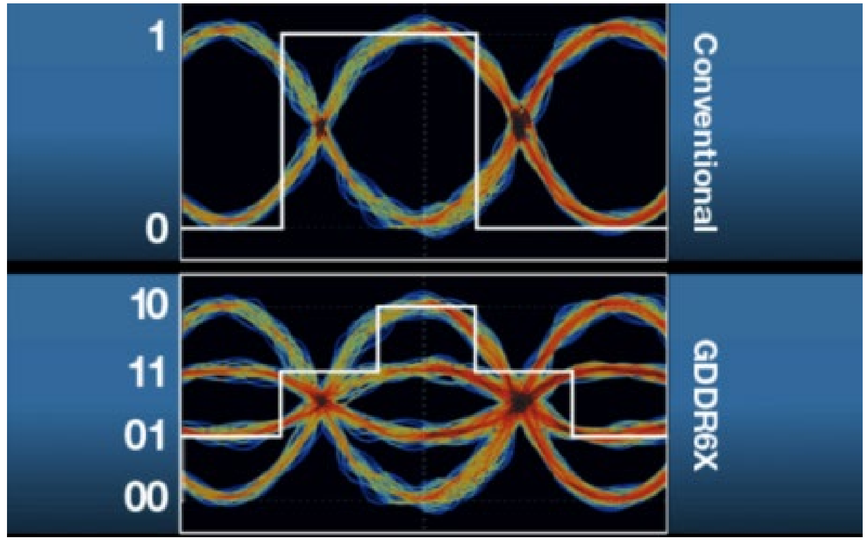




Advanced Packaging SoC Wafer Sort Test Challenges

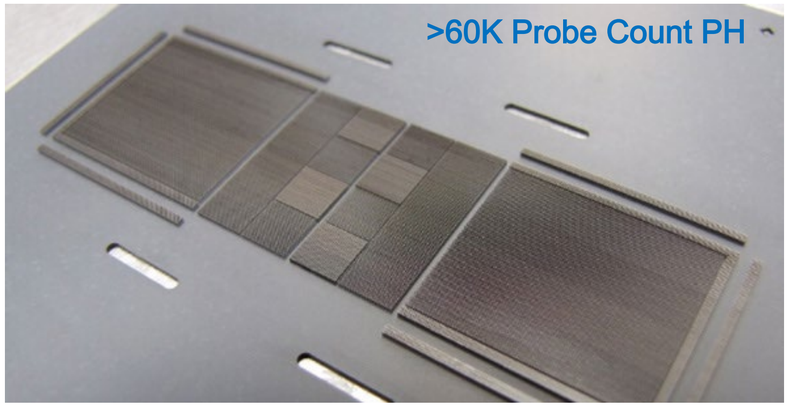
- **Advanced Packaging Drive Large Probe Count Design**
  - Multiple IC and HBM integration and communication drives large bump count
  - AP device in order of 1K~5K probes per die → Advanced Packaging SoC on 15K ~ 60K probes per die
  - Large probe count drive low probe force requirements
  - High Performance Computing (HPC) require higher probe current carrier capacity
- **Advanced Packaging Device Required High Speed Test**
  - HBM GDDR6x speed requirement reach 8GHz
  - GPU data communication interface transition to PCIe6 64Gbps (NRZ 32Ghz, PAM4 16GHz)



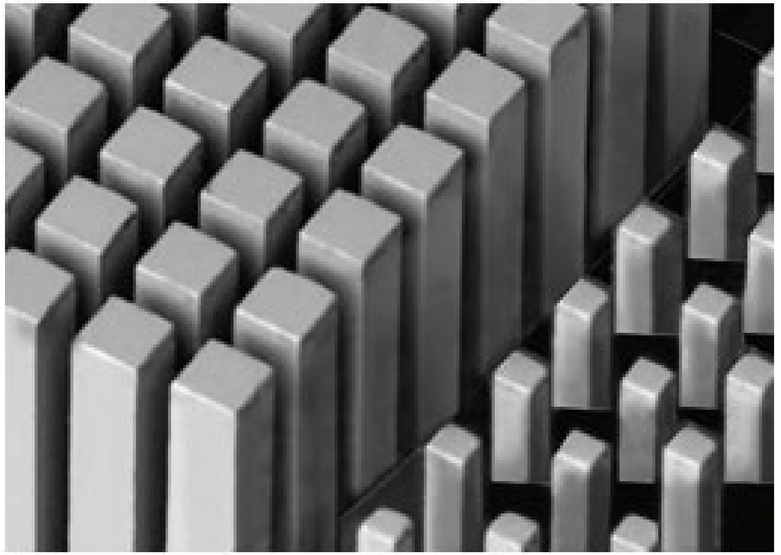


Apollo MEMS Probe Card for Advanced Packaging SoC Bump Testing

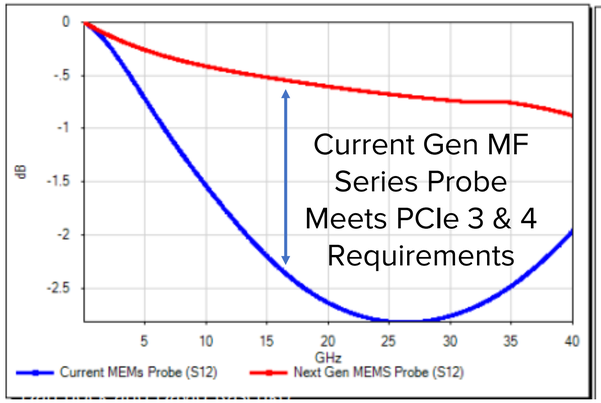
- **Apollo MEMS Probe Card Offers**
  - Low probe force large probe count solution
    - Probe force <3gf, production proven >65K pin count design
  - Wide Range of Probe selection and offer hybrid probe head solution
    - Use large probe on power net with enhanced CCC feature
    - Use thin probe for signal net with high-speed feature
- **Next Generation MEMS Technology Probe for High -Speed Test**
  - Short probe enable small inductance
  - >-0.5 dB insertion loss at 16GHz (PCIe 5 and 6)
  - <-15 dB return loss at 16GHz (PCIe 5 and 6)



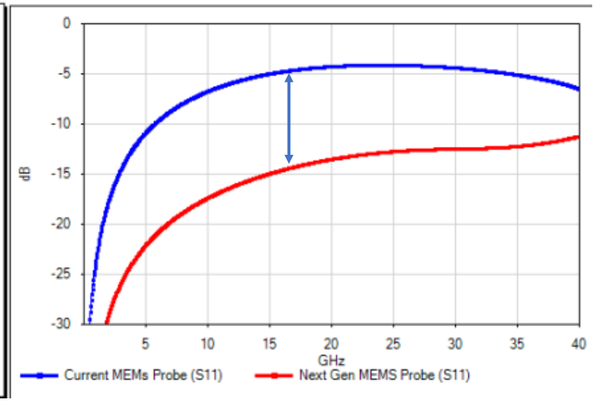
Hybrid Probe Head



Insertion Loss

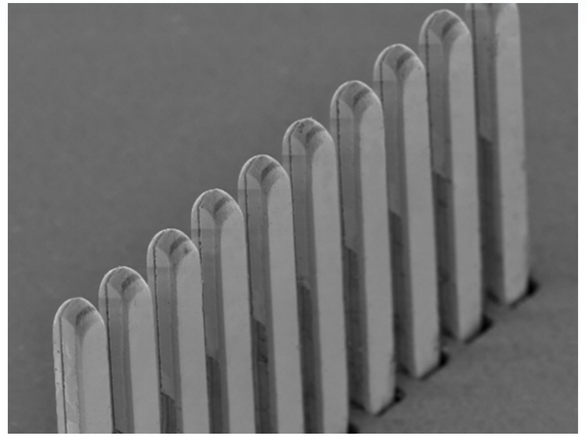


Return Loss

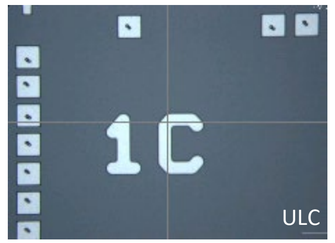


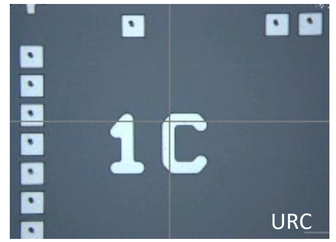
Kepler MEMS Probe Card for Advanced Packaging SoC PAD Testing

- **Kepler MEMS Probe Card Offers**
  - Sacrificial PAD probing on Advanced Packaging SoC Die
  - Wide temperature range at large active area
    - 190°C temperature range over 75mm active area
  - Low probe force for large pin count scalability and minimize PAD damage
  - Wide Range of Probe selection for different Advanced Packaging device testing need:
    - MF45: fits HBM and HBM2 layout
    - MF60: fits HBM3 layout
    - MF80: fits CoWoS sacrificial PAD layout, support Cu Pad testing
    - MF130: fits most of HPC and GPU PAD layout, 1.5A CCC



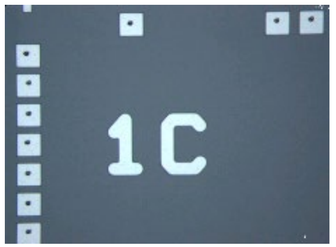
MF60 Radius Tip Probe

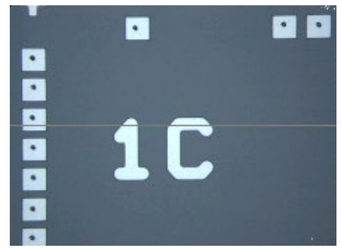




Dual Temp -40°C ~ 150°C
Over 72mm AA Probe Mark

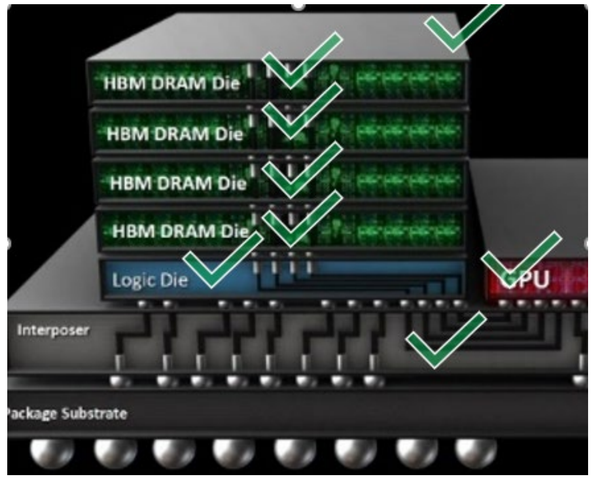
72mm





Summary and Key Takeaways

- **Advanced Packaging Demand more Test as It's Volume and Complexity Increasing**
  - Advanced Packaging IC revenue continues growing since 2014, forecast maintain 6.6% CARG until 2025
  - Advanced Packaging complexity grow exponentially, industry facing low package yield and high packaging cost challenge
  - Industry demanding test solution to test all components to improve final yield and reduce packaging cost
- **FormFactor Has Production Proven PC Solution to Test Each Component in Advanced Packaging**
  - Matrix HFTAP PC for KGD and HBM KGS test
  - Altius PC for HBM KGSD and Si Interposer test
  - Apollo MEMS PC for SoC CuPillar with solder bump test
  - Kepler MEMS PC for SoC PAD testing



THANK YOU