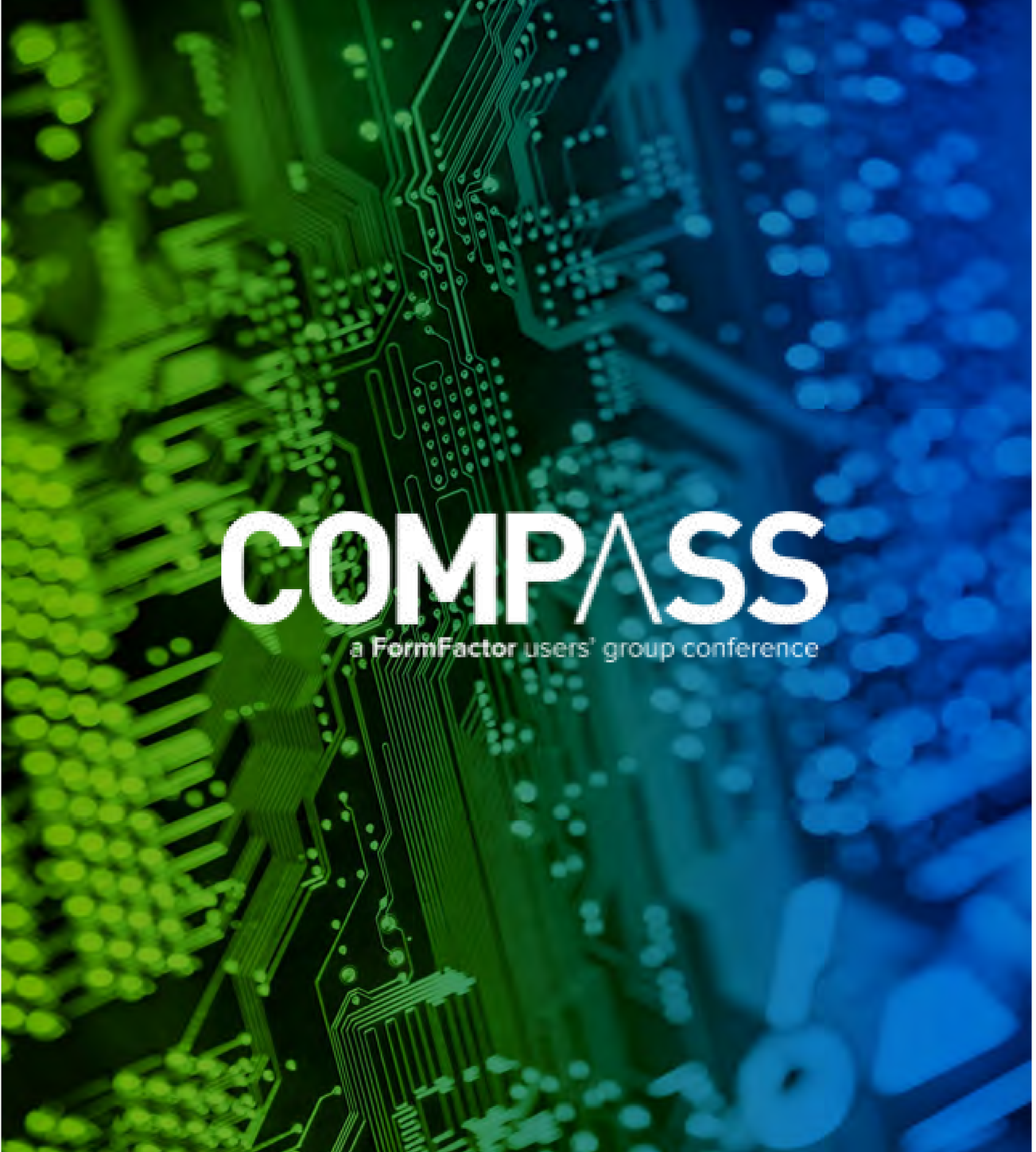


Characterization of 1/f noise at wafer level, using CM300xi-ULN

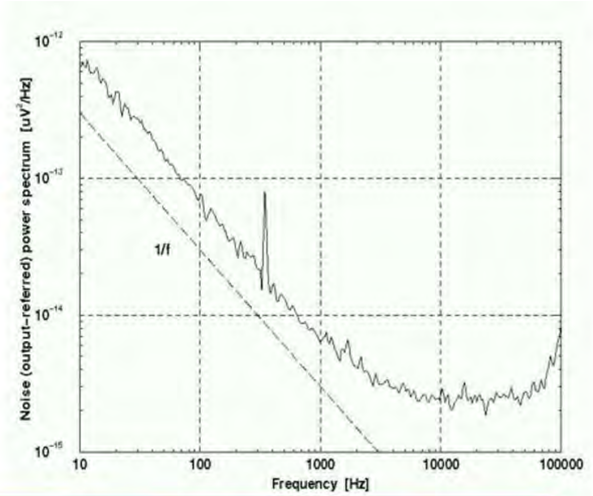
Authors: Fausto Simioni, Lorenzo Labate

Importance of 1/f noise characterization

- ST products in several categories (HDD drivers, audio amplifiers etc.) are becoming more and more demanding in terms of noise performances, so an extensive characterization of 1/f noise must be performed on almost each kind of device we make available to designers through our design kits: MOS, BJT, resistors, diodes etc.

- As an example, 1/f noise in CMOS is defined as shown to the right.

CMOS transistors noise (power spectrum) exhibit a **1/f behavior** at low frequencies



Main noise source: random trapping and detrapping of carriers in the oxide traps **[1]**

Fluctuations of current due to carriers population fluctuations

Fluctuations of mobility due to occupied oxide traps number fluctuations:

$$\frac{1}{\mu} = \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{TR}} = \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}} \pm \alpha \cdot N_T$$

other contributes to mobility

oxide traps contribute

occupied traps per unit area

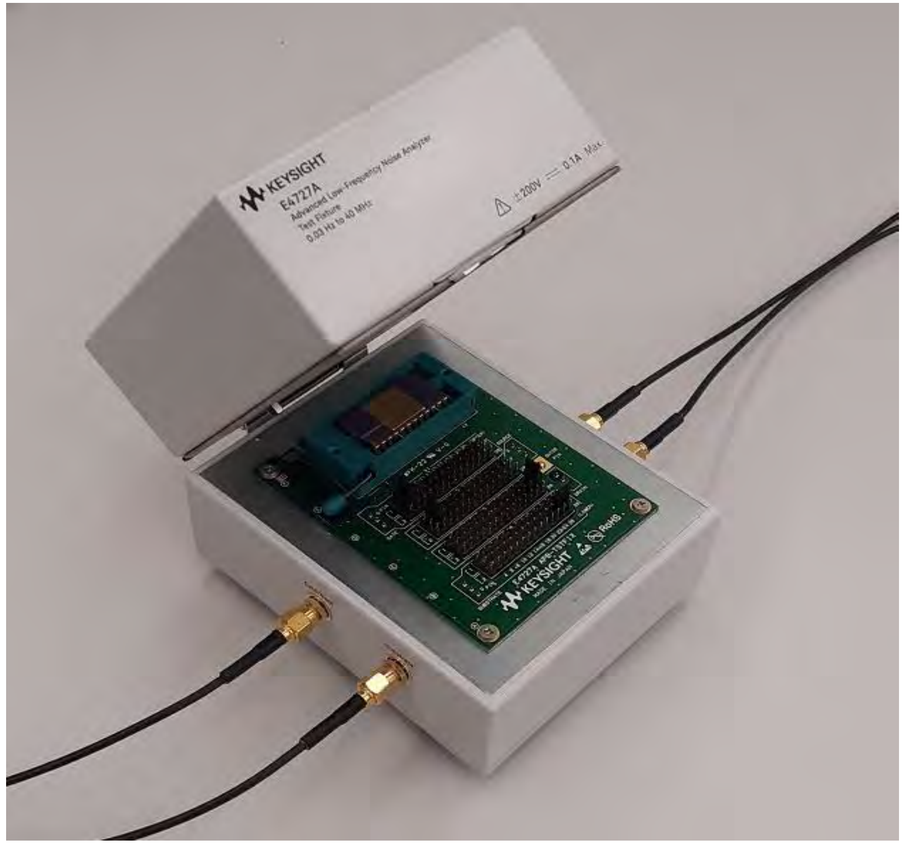
[1] K.K. Hung et al., IEEE Trans. El. Dev., ED37 (1990), p.654

1/f Noise Characterization Before CM300xi-ULN

1/f noise characterizations before CM300xi-ULN - 1

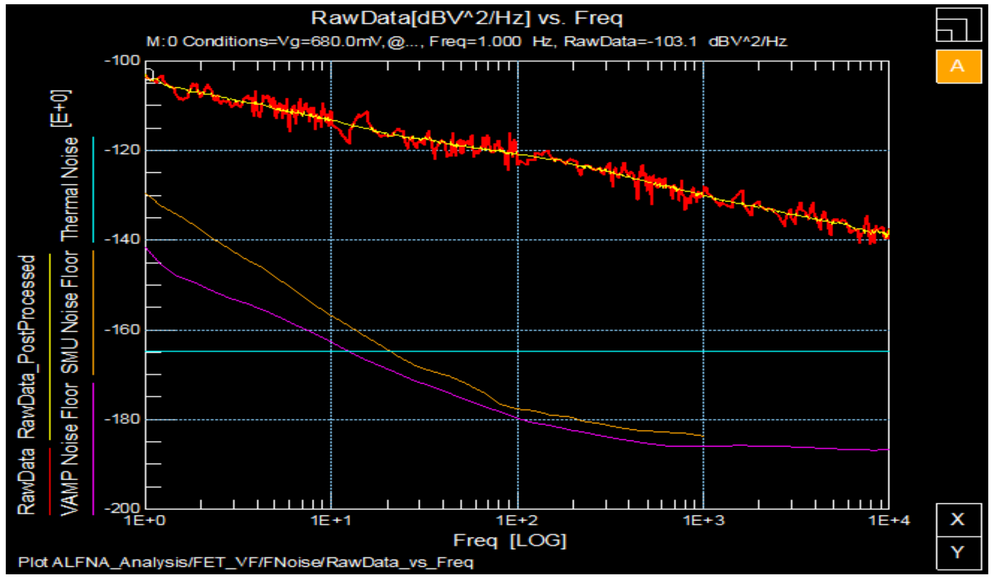
- Due to the limitations of standard probers in terms of noise performances, 1/f noise characterizations at low overdrive values, especially on low noise CMOS, had to be performed at package level inside a shielded fixture (provided with the Keysight E4727A system).

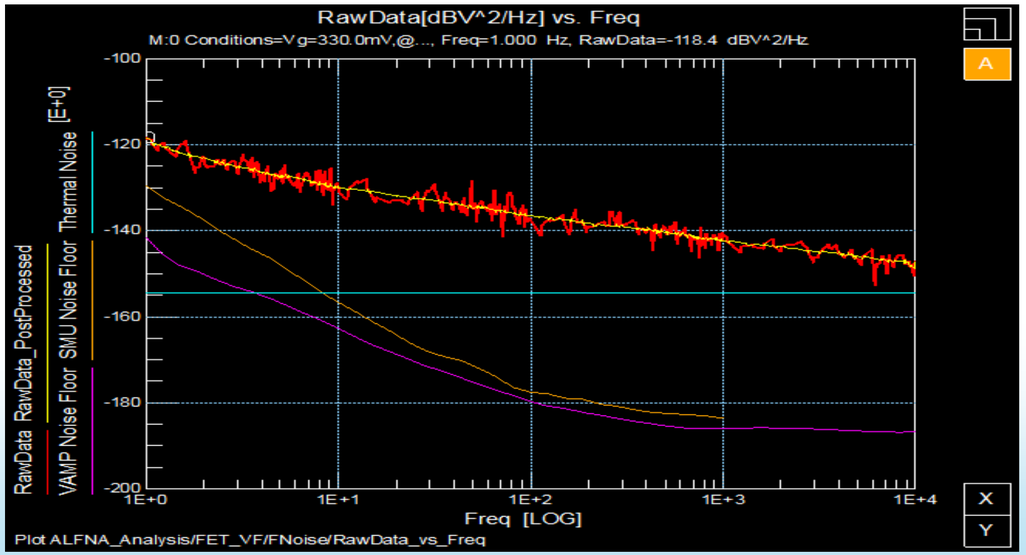
- The noise floor of this kind of setup is low enough to allow the measurement of 1/f noise at the minimum overdrive of interest, even for low noise CMOS.



1/f noise characterizations before CM300xi-ULN -2

- Before the adoption of the FormFactor CM300xi-ULN probe station, 1/f noise characterization was subject to the limitations shown in these plots.
- Measurements at wafer level could properly detect values as low as -105dB^2/sqrt(Hz)@1Hz.
- Measurements at package level could go as low as -120dB^2/sqrt(Hz).





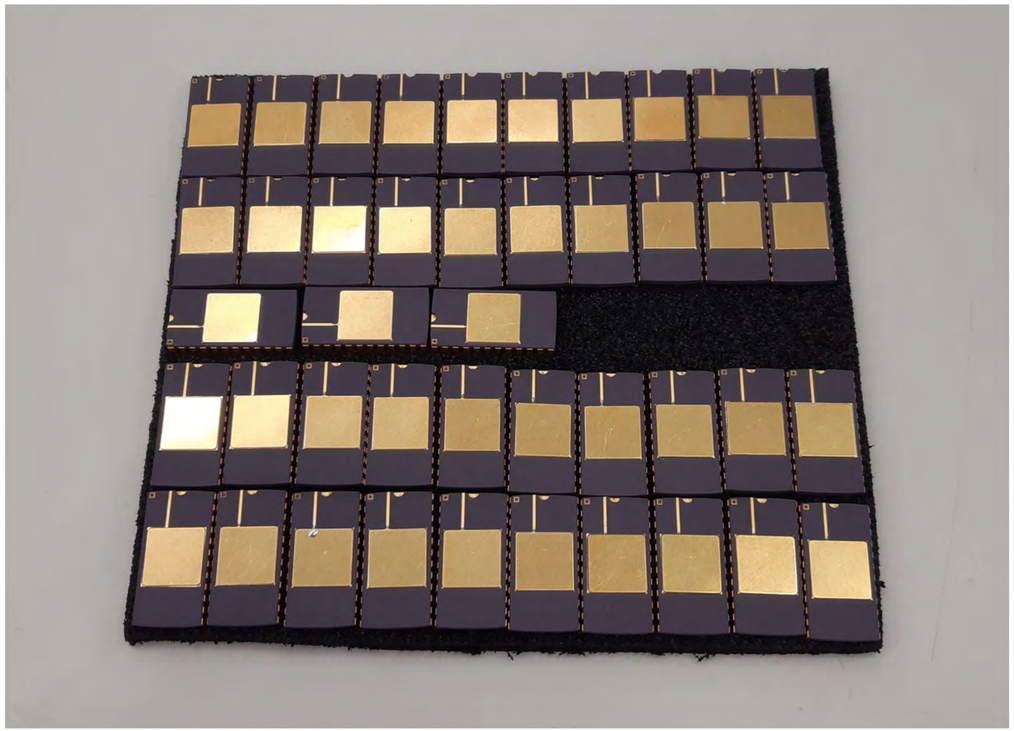
Package level characterization drawbacks

Characterizations done at package level have some drawbacks:

1) Time: prior to performing the actual 1/f characterization, samples have to be assembled, thus requiring the preparation of assembly documentation and bonding diagrams, moreover, it can take up to two weeks before packaged samples are made available by the assembly line, depending on the queue.

2) Limited temperature range: only a characterization at ambient temp can be performed, since the shielded fixture isn't thermally controlled.

3) Limited possibilities to gather statistical data: measurements are performed manually switching samples one by one.



Challenges of MOS 1/f noise characterizations

- As previously mentioned, MOS transistors used in some products work at very low Vgs voltages, even as low as threshold voltage, this requires to perform 1/f noise characterizations at several overdrives (OD=Vgs-Vth), starting from OD=0V.

- This is a very challenging task to be achieved at wafer level, it requires a prober specifically designed and installed with noise performances in mind, otherwise you can experience an erratic behavior of the 1/f slope, which, ideally, should decrease one decade in amplitude every two decades in frequency.

FormFactor CM300xi-ULN System Installation

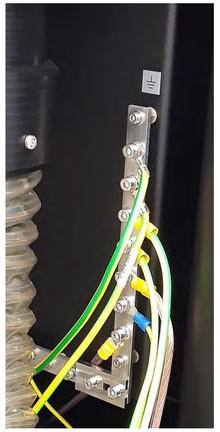
FormFactor CM300xi-ULN installation

- The FormFactor CM300xi-ULN probe station has been recently adopted as the prober of choice for low noise characterizations, due to its noise dedicated features and promising specs.

- Lorenzo Labate, as the Castelletto ST electrical characterization lab manager, supervised the whole installation of the system by FormFactor technicians, starting with a mechanical and electrical ambient noise evaluation, prior to the system installation, in order to evaluate the goodness of the environment chosen for the system placement.

Probe station chamber noise floor evaluation - 1

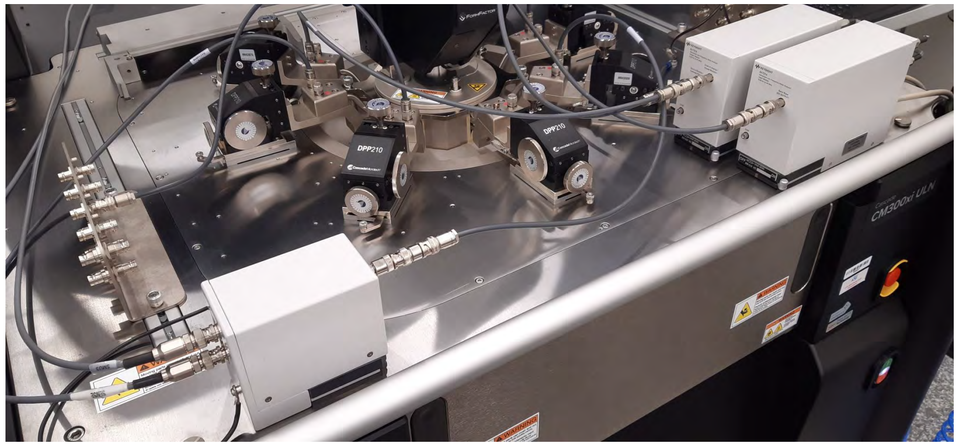
- Fausto Simioni, as the person in charge of 1/f noise characterizations, performed a 1/f noise floor evaluation after the system installation, using the Keysight E4727A system.
- Each instrument involved in the noise floor measurement (parameter, noise analyzer) had the ground connected to the probe station rear ground connectors and each of the Keysight E4727A modules ground have been connected to the prober plane chassis. Also, each additional instrument has been plugged into the filtered PSU provided with the system.



CM300xi-ULN

Rear Ground Connections

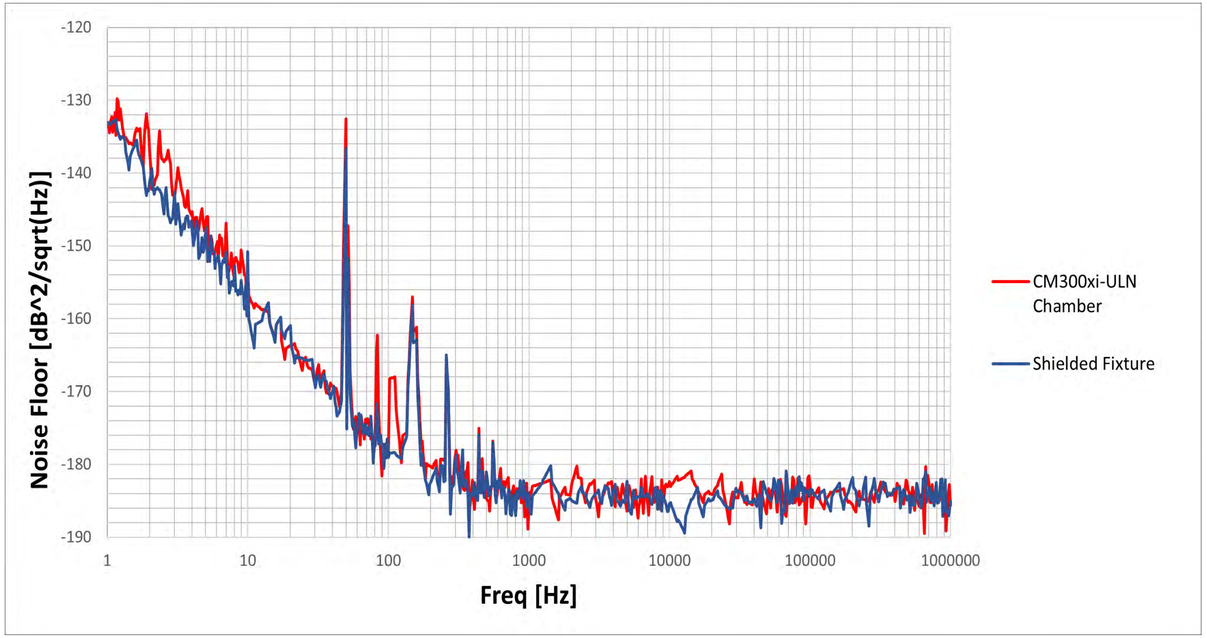
Keysight E4727A Input/Output Modules Placement



Probe station chamber noise floor evaluation - 2

- The probe station chamber noise floor evaluation results show that the system noise floor level is at least comparable with the results achieved inside the shielded fixture, used in packaged devices characterizations, and allows us to take full advantage of our Keysight E4727A system capabilities (-130dB^2/sqrt(Hz) @1Hz).

- A small group of 50Hz harmonics is still present, both in the shielded fixture and the probe chamber, further tweaking of cables and ground connections could solve that, but even as it is, they are so limited that don't compromise the goodness of our 1/f noise measurements, what matters is the floor level, single harmonics can be removed in postprocessing.

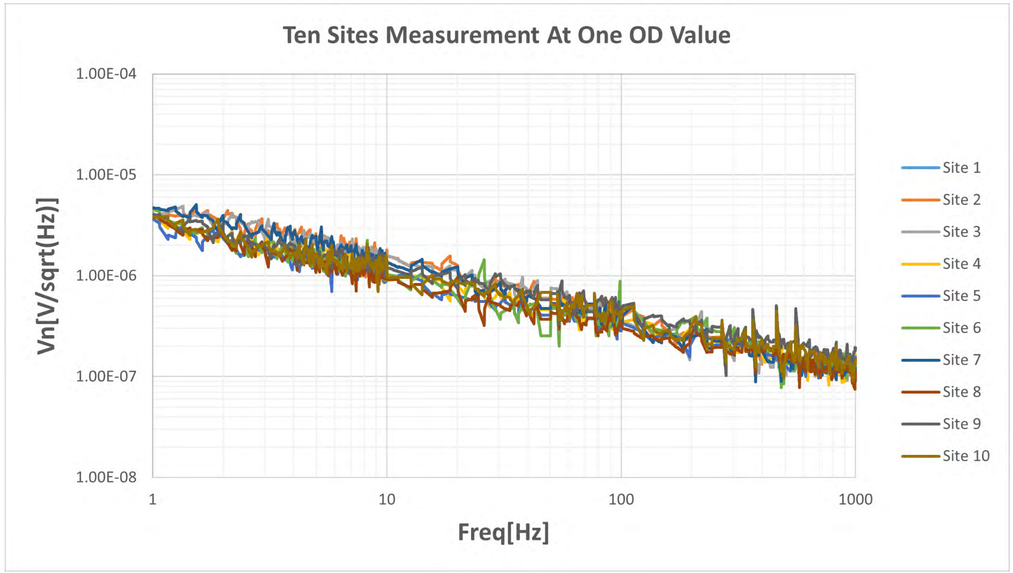


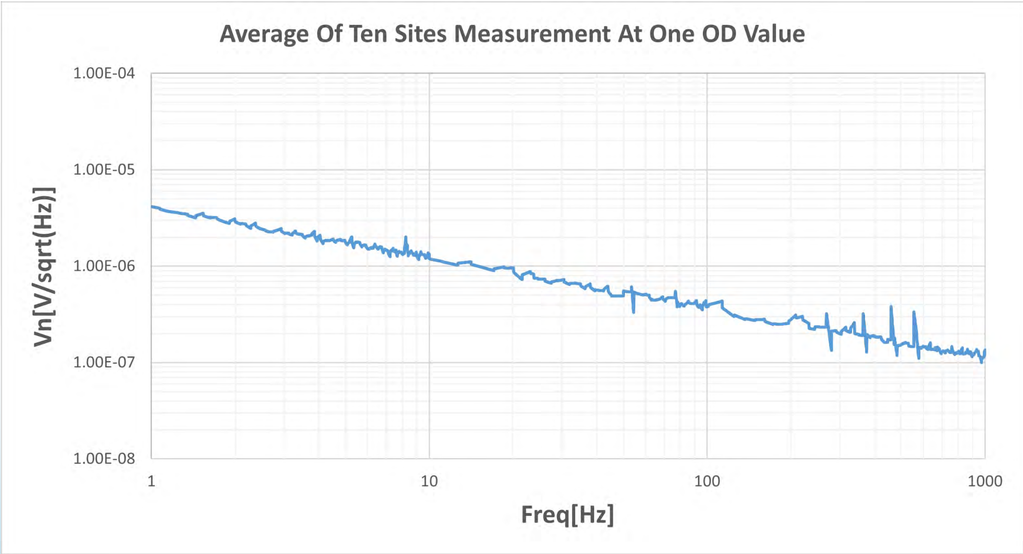
A Real Life Case

1/f noise characterization of 1.8V CMOS - 1

- An investigation of differences, in term of noise performances, detected in a product transferred from a technology to another one (following as technology 1 and 2), has been conducted on 1.8V n-ch MOS transistor, 130nm lithography. Urgency was a key factor in investigating the potential issue.

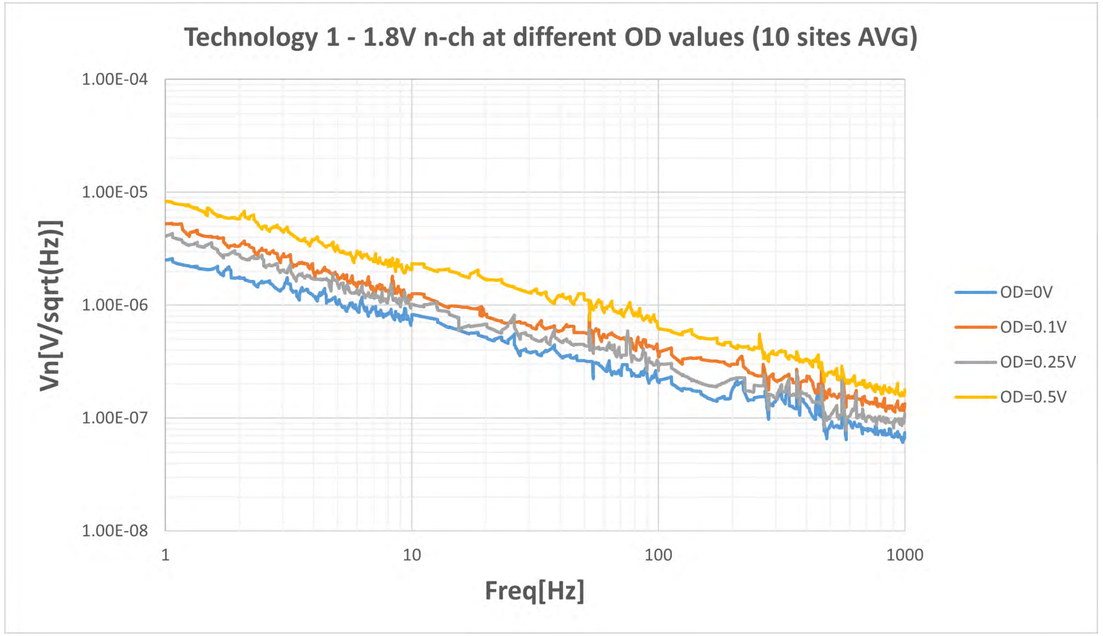
- Two wafers have been evaluated, one for each technology, and, on each wafer, ten sites have been measured at OD=0V, 0.1V, 0.25V, 0.5V. On the right, an example of a ten site 1/f noise measurement at one OD value on one kind of CMOS can be seen, from this batch of ten measurements, the average is calculated to obtain one single trace at each of the 4 OD levels and used for comparison purpose between technologies.





1/f noise characterization of 1.8V CMOS - 2

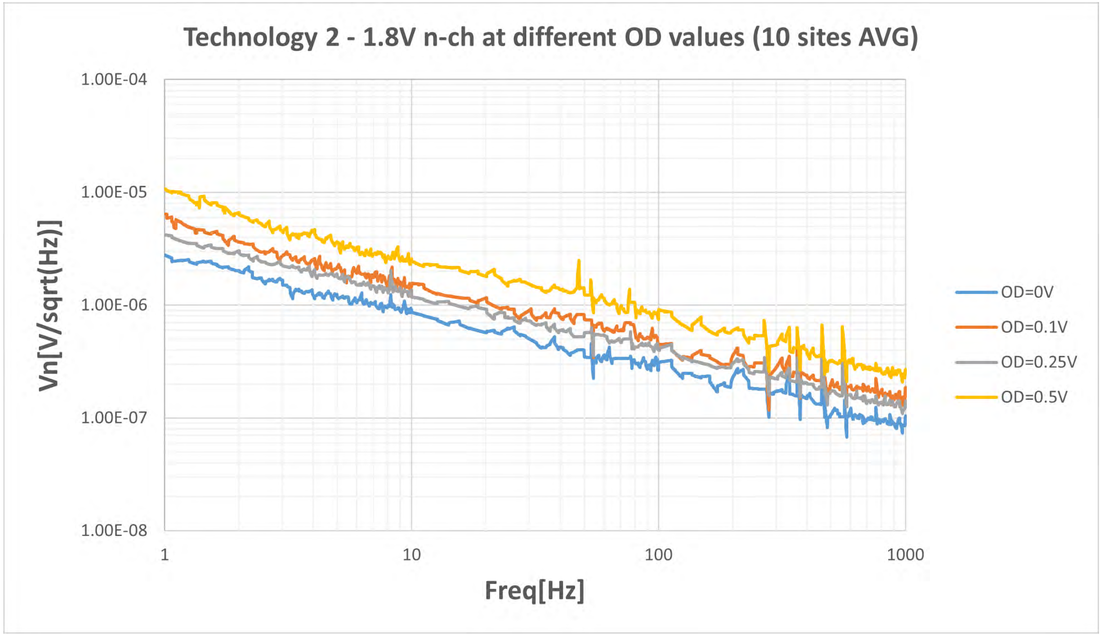
- We knew what to expect from the measurements on technology 1 CMOS, since a characterization at package level had already been conducted a few years back.
- The plot shows the noise scaling at the four different OD values, each of the four traces has been extrapolated by performing the 10 sites average explained in the previous slide.
- Results at each OD value are in line with expectations, based on a characterization previously done at package level, and even at the lowest overdrive value, the 1/f noise slope is clean and in line with the theoretical 1/f noise expected behavior. In terms of raw data, the 0V overdrive trace is close to -120dB^2/sqrt(Hz) @1Hz.



1/f noise characterization of 1.8V CMOS - 3

- 1/f noise of technology 2 had never been evaluated in the past, so a characterization was needed to confirm or deny that the difference in terms noise performance detected in a product was indeed coming from the shift from one technology to the other one.

- As for technology 1, also for technology 2 the measurements resulted clean at every OD level and in line with the theoretical 1/f noise expected behavior.



1/f noise characterization of 1.8V CMOS - 4

- For comparison purpose, the noise value at 1Hz is extrapolated, this is done by multiplying each of measurement points for the square root of the corresponding frequency and then performing an average. Based on this value, the PSD square root normalized coefficient (Kf) is calculated.

- The table shows a comparison between the Kf values for both technologies. No significant differences can be observed, so the switch from technology 1 to technology 2 doesn't seem to be the root cause of the noise performance difference observed at product level.

Vgs-Vth [V]	Technology 1 1.8V n-ch MOS Kf [µm*µV/√Hz] Wafer char.	Technology 2 1.8V n-ch MOS Kf [µm*µV/√Hz] Wafer char.
0.0	8.53	8.91
0.1	10.62	11.64
0.25	13.14	14.60
0.50	22.3	25.1

Vn@1Hz=AVG(Vn*sqrt(Freq))

Kf=Vn@1Hz*sqrt(Area)

Conclusions On CM300xi-ULN Wafer Level Characterization And Future Steps

Pros Of CM300xi-ULN Usage In A Real Case

- Being able to perform this characterization at wafer level, thanks to the CM300xi-ULN probe station adoption, allowed us to complete this urgent investigation in a matter of a few days, compared to a few weeks, which typically is the time required for a characterization at package level, considering also the time required for package assembly.

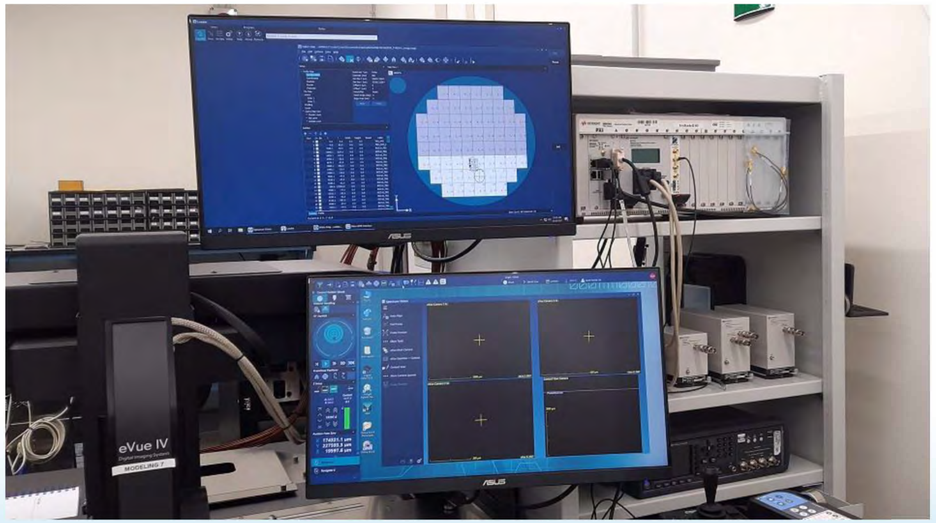
- Since this real life scenario was concerning a potential problem detected on one of our products, the speed in collecting conclusive data was a key factor.

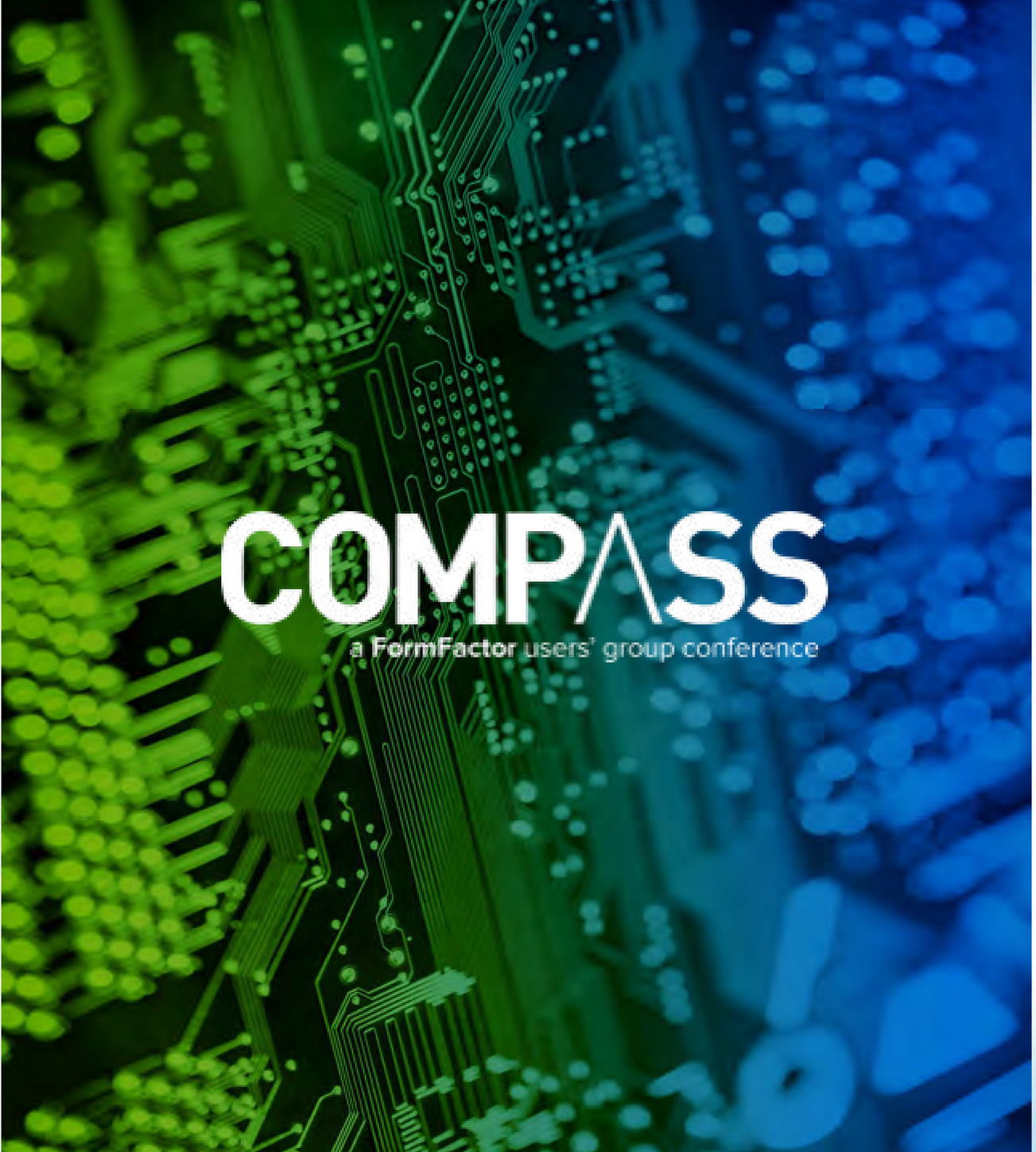
Future of 1/f noise characterization at wafer level

The next steps in 1/f noise characterization at wafer level made possible by CM300xi-ULN include:

1) Noise measurements in temperature, ranging from -40C to 175C.

2) Full wafer map statistical noise measurements for noise spread evaluation. In order to perform this, an update of the noise measurement software of the Keysight E4727A is required.





THANK YOU