Next Generation, Fine Pitch HBM Cube Characterization to Production

November 17, 2020

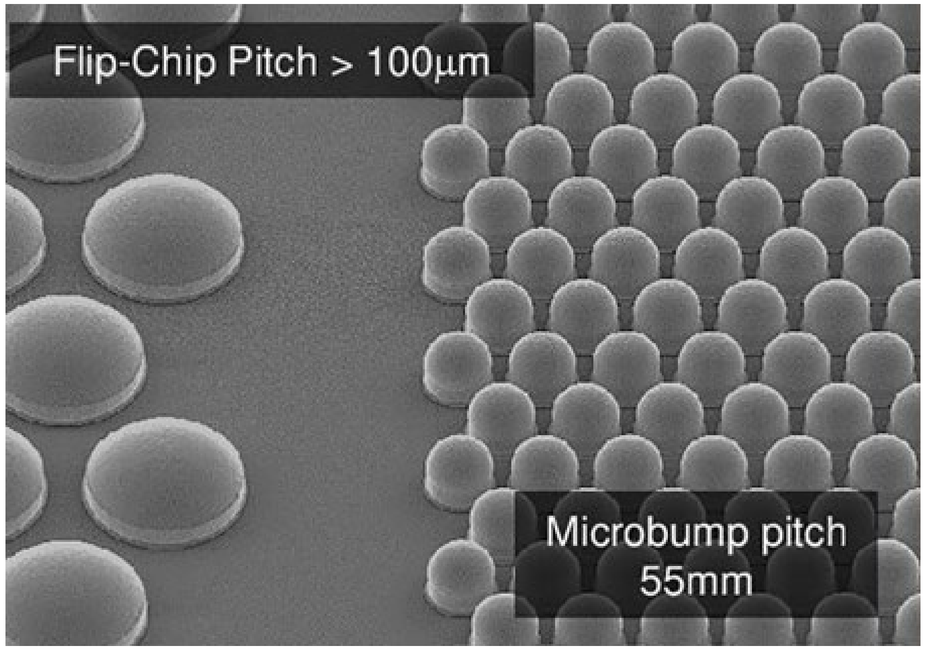
Quay Nhin

Agenda

- Follow up on last year HBM paper- probing complexity and challenges
- HBM test insertions- cost and coverage
- Vertical solution status on direct access µ-bump probing
- Call to action for upcoming next generation HBM3/HBMnext

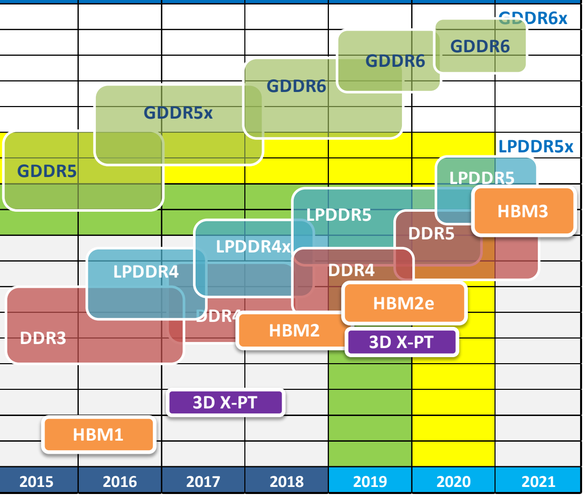
How Does Advanced Packaging (HBM) Impact Test?

Complexity!

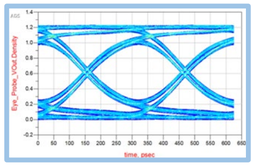


ATE Tester + Probe Card + Wafer = Data Eye

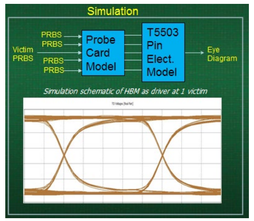
FFI Product Platform	FFF HFTAP Product Class	Clock (MHz)	Data Rate (Mbps)
		9000	18000
		8000	16000
		7000	14000
		6400	12800
		5600	11200
Matrix	K40	4267	8533
		3733	7466
Matrix	K32	3200	6400
		2800	5600
Matrix	K22	2134	4267
		1867	3733
Matrix	K16	1600	3200
Matrix	K12	1339	2677
Matrix	K10	1067	2133
		933	1866
Matrix, PH	K8	800	1600
		667	1333
Matrix, PH	K5	534	1067



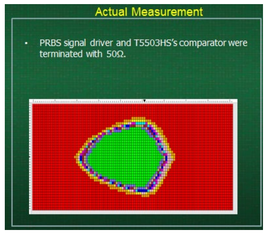
Simulation



Measurement



Device validation



Spatial/Mechanical – Higher Density

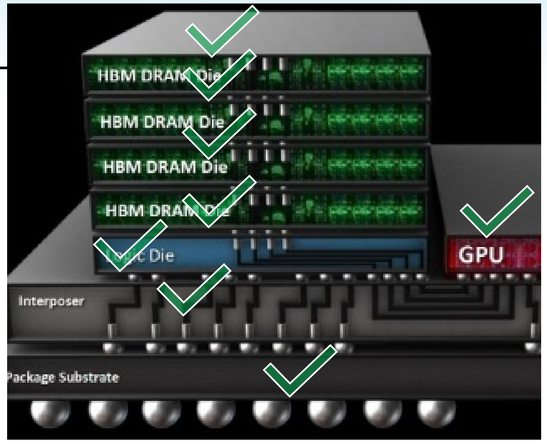
- Smaller pitches and higher probe counts
- More delicate contacts (new materials)

Electrical – Higher Performance

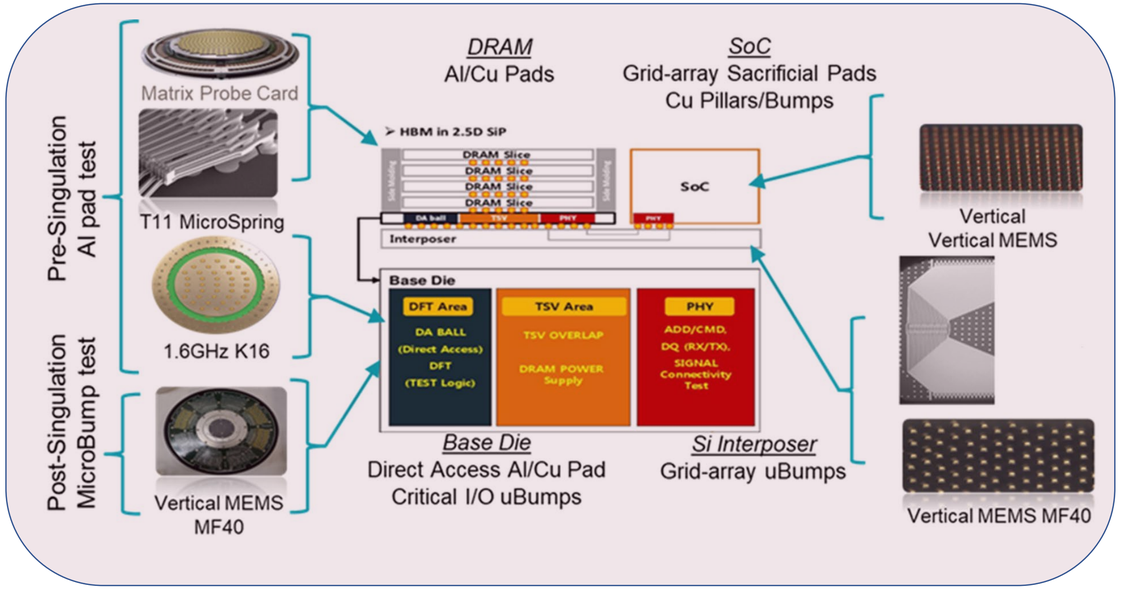
- Higher clock speeds, nearing RF frequencies
- Increased current per contact, higher power density

How Does Advanced Packaging Impact Test?

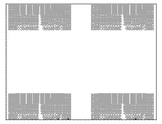
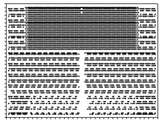
Cost, Complexity, and Coverage!

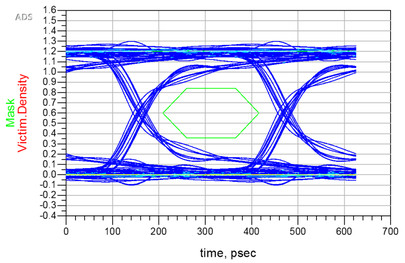


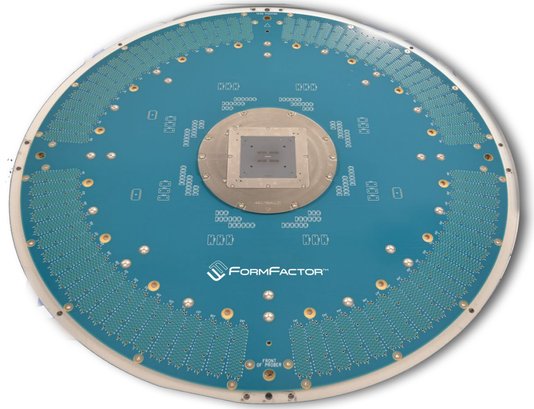
- **Final test of assembled package is necessary, but provides limited insight to improve performance and yield**
  - Wafer test provides valuable yield learning on component die and ensures the final stacked assembly does not get scrapped because of one bad die
- **Ideally, each component is good before integration**
  - Nirvana is Known Good Die (KGD), just test everything
- **Economics may dictate something shy of KGD**
  - Pre-package wafer test is fundamentally scrap-cost avoidance
  - Final-test and system-test opportunities prevent escapes
- **Cost vs. coverage optimization comes down to math**
  - Compromise = Probably Good Die (PGD)
  - Hedge bets – e.g., design interposers/ bridges with redundant vias, and build repairability into each HBM sub-die
  - Balance test coverage to catch higher-probability/impact issues, while accepting risk of lesser issues slipping through to final test

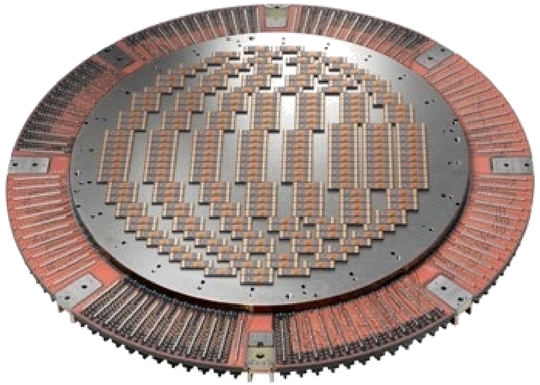


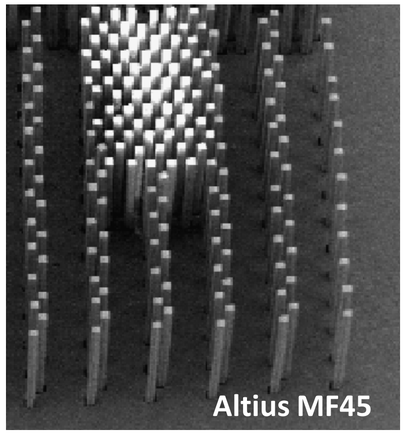
HBM Probing Solution Status for Pad and Direct Access µ-bump

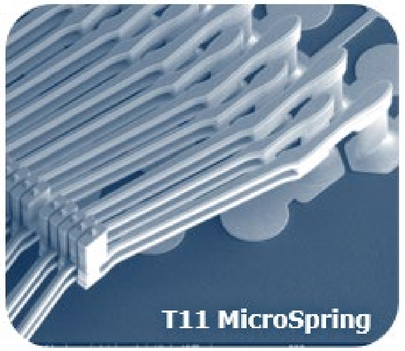
HBM Probe Solution	DUT Config	PC pin count	Operating Frequency	Status
Vertical (µ-bump)	 x4	~15,000	1.6GHz/3.2Gbps	Qualified!
	 x1	~5,350	1.6GHz/3.2Gbps	Qualified!
Sacrificial pad	up to x64	~20,000	3.2GHz/6.4Gbps	Qualified!











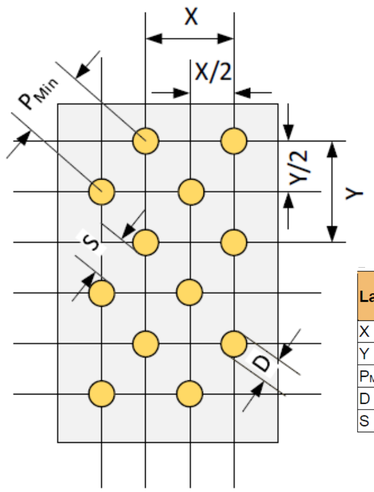
FormFactor™

PCB and MLO design and manufacturing supports up to 1.6GHz and 3.2GHz

Next Gen HBM3/HBMnext in Feasibility Study

- HBM3/HBMnext on the horizon and JEDEC is firming up on the final specification
  - **73um minimum stagger µ-bump pitch**
  - **Testing of live HBM cube up to 8Gbps (4GHz)**
  - **Sacrificial pad testing of high parallelism mass production sort up to 8Gbps at wafer-level**

- Multi-suppliers and customer collaboration needed to ensure success



Label	Nominal Value	Description
X	96µm	Horizontal pitch of two adjacent micro bumps
Y	110µm	Vertical pitch of two adjacent micro bumps
P_{Min}	73µm	Minimum pitch of the bump field
D	28µm	Micro bump Pillar Diameter
S		Bump to Bump air gap; S = P_{Min} - D

THANK YOU