Solutions to Multiple Probing Challenges for Test Access to Multi-Die Stacked ICs

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CMOS Scaling…

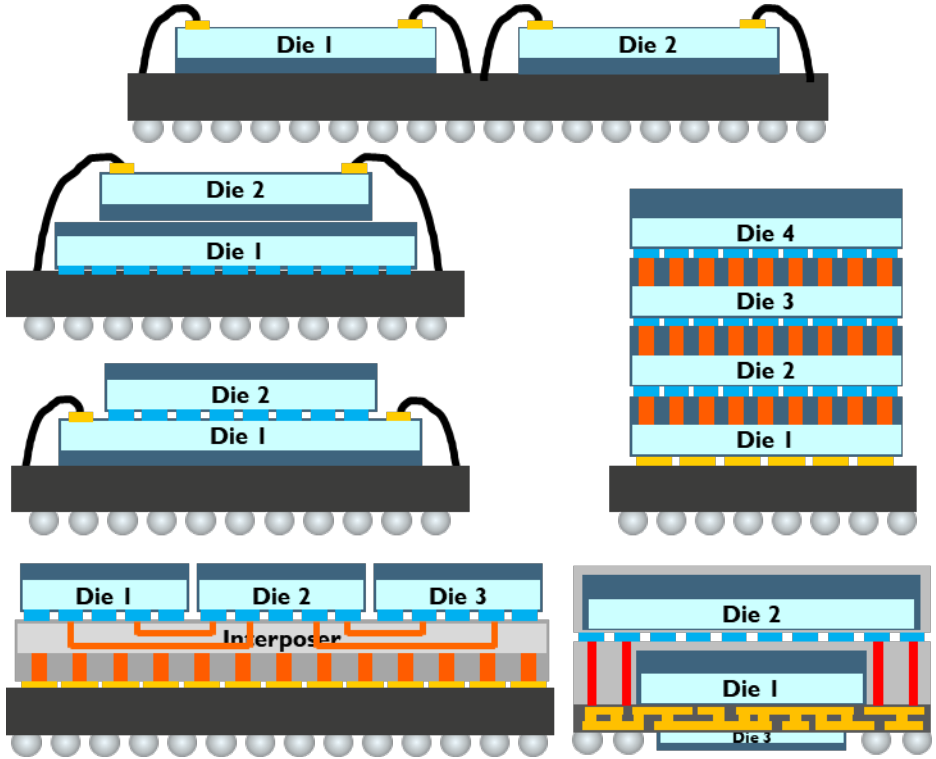
- **CMOS Scaling Continues**
  - But requires increasing investments
  - Only few companies can afford this
  - … And one day, it <u>will</u> stop!

First EUV stepper
world-wide in use at imec

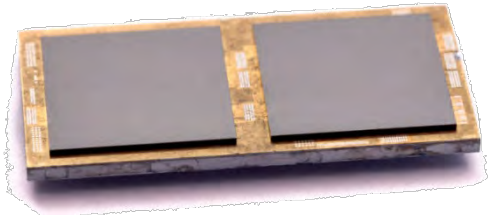
CMOS Scaling... ...Assembly & Packaging

Baton Pick-Up by Innovations in

- **Multi-Die Stack-Assembly**
  - Package-on-Package / Die-on-Die
  - Side-by-side and vertical stacking
  - Micro-bumps, TSVs; wafer thinning
- **Advanced Packaging**
  - Flip-chip, Through-Package Via (TPV)
  - Redistribution layers
  - Integrated passives and interposers
  - Wafer-level fan-out and packaging



Testing of Multi-Die Stacks



- **Test Stages**

  External Test Access

  1. Pre-Bond Test : prior to stacking
  2. Mid-Bond Test : incomplete, partial stacks
  3. Post-Bond Test : complete stacks, prior to packaging

  } probe technology

  4. Final Test : complete, packaged stack

  } test socket

- **Test Flow Optimization**
  - Too much vs. too late testing
  - Optimization with 3D-COSTAR: http://www.ce.ewi.tudelft.nl/3dcostar
- **Test Access**
  - Internal: 3D-DfT (e.g. IEEE Std 1838™-2019) and External: probing + socket

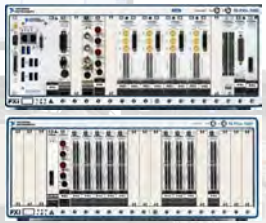
‘Vortex-2’: FormFactor CM300 Dual Config Station

FormFactor™

- Adapted CM300 probe station with thermal control

National Instruments™

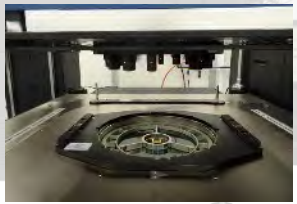
- Parametric & functional
- Micro-bump probing with ultra-wide switch



STS T2

Reid Ashman

- Manipulator
- Docking interface



Presentation Outline

1. Introduction
2. Probing on Large Tape Frames
3. Probing on Ultra-Thin Wafers on Tape
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5. Probing Dense Arrays of Micro-Bumps
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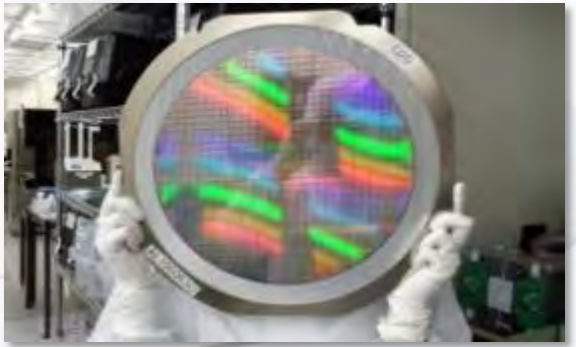
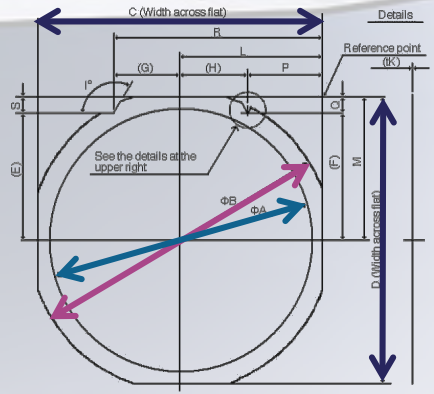
7. Case Study
8. Conclusion

Challenges and Solutions

Multi-Die Stack-Assembly Flows use Tape Frames

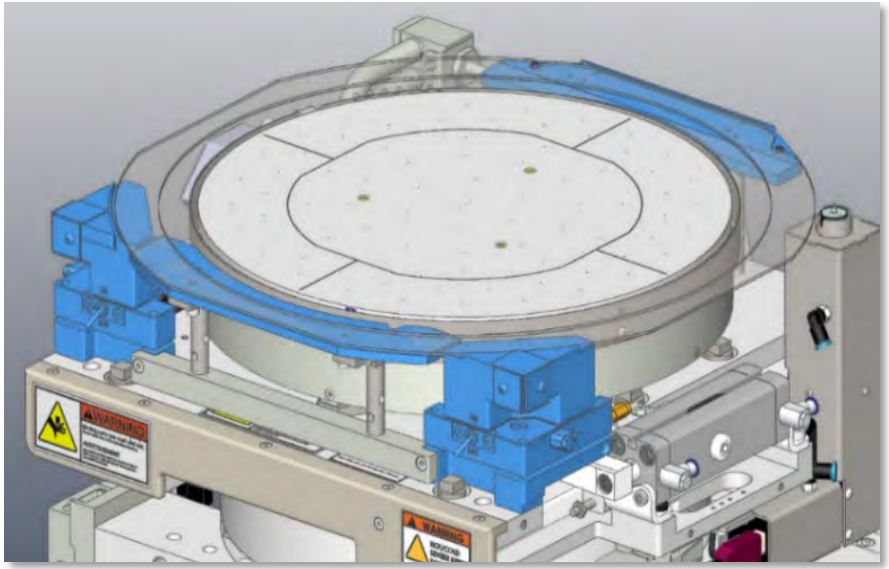
- **Tape Frame Serve as Temporary Carrier for**
  - Diced wafers
  - Ultra-thin wafers
  - Pick-n-placed dies and die stacks [Marinissen et al. – ITC'15]
- **Tape Frame Specifications**
  - Larger than the wafer it must hold
  - SEMI Standard G74-0669:
    - ↔ Inner diameter : 350mm
    - ↔ Outer diameter : 400mm
    - ↔ Width across flat : 380mm



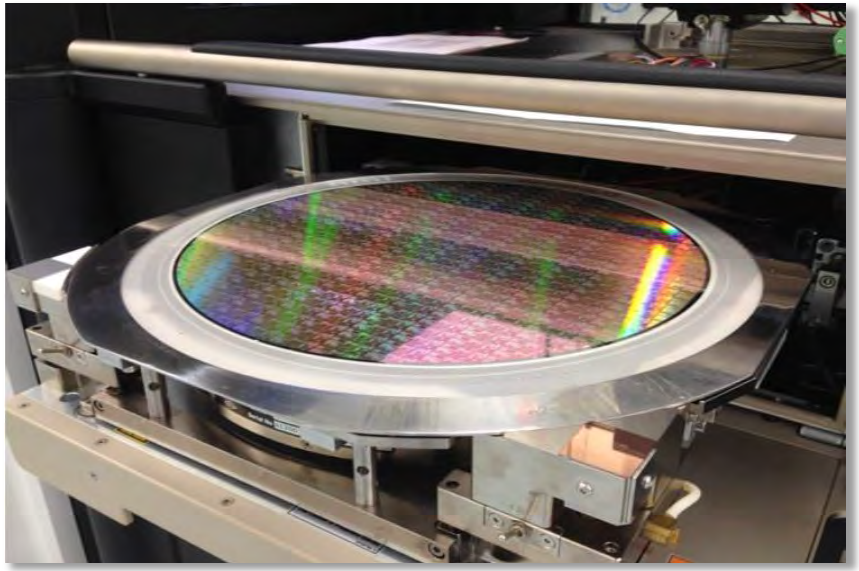


FormFactor CM300 Handles Large Tape Frames

- Adapted chuck for manual loading through front-port of SEMI Std G74-0699 tape frames



- Extra maneuver space for chuck
- Chuck camera away from chuck
- Extra support bars for large frames



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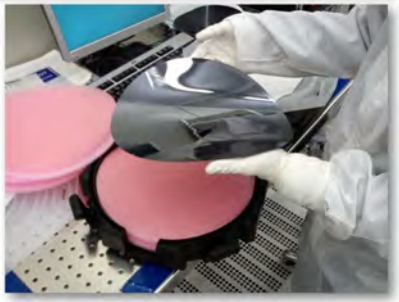
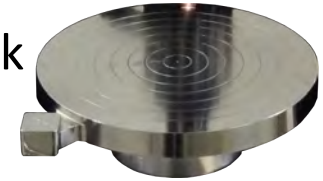
Multi-Die Stacks use (Ultra-)Thin Wafers

- **Wafer Thinning down to**
  - 200µm: to fit stack in package cavity
  - 50µm: to expose TSVs
- **Ultra-Thin Wafers Sag, Bend, and Curl**
  - Require mechanical support
    - Carrier wafer: silicon, glass
    - Frame with UV-curable dicing tape
  - Temporary bonding → debonding
- **Probing Challenge**
  - Probing on flexible ultra-thin wafer on flexible/stretchable dicing tape



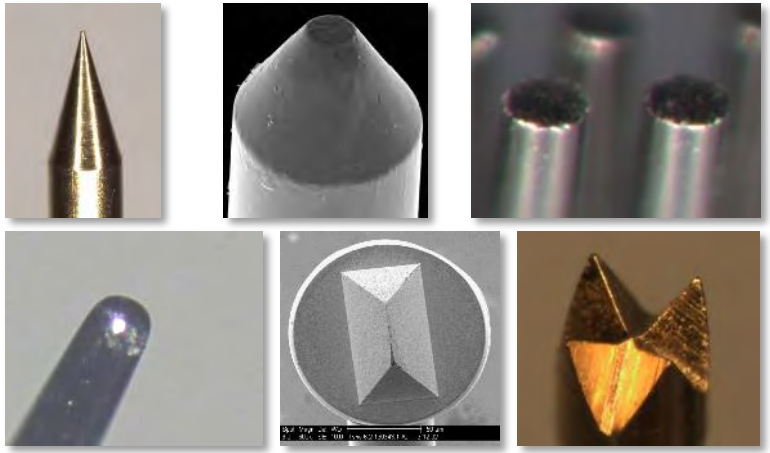
Probing Requires Probe Force on Probe Target

- **Objective 1**: good electrical contact
  - Measure: contact resistance R_C
  - Wafer chuck over-travel
  - Consequence: probe mark

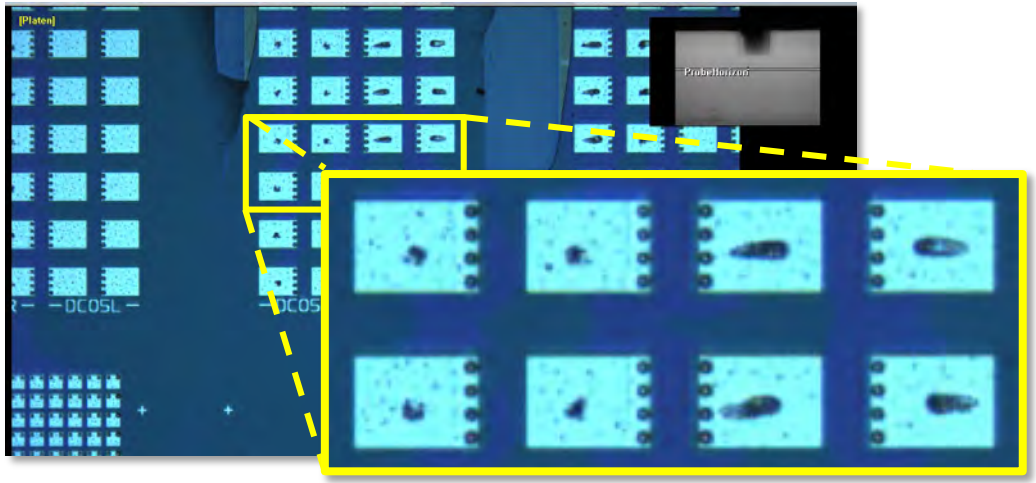


- **Objective 2**: minimal impact probe mark on other function(s) of probe target
  - Measure: probe mark area as percentage of probe target area

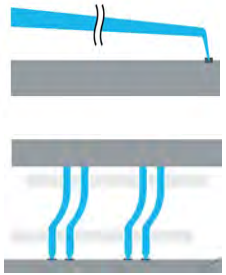
- **Probe Mark Determined by**
  - Metallurgy of probe target
  - Probe concept: cantilever, vertical, MEMS
  - Probe tip: metallurgy, shape
  - Chuck over-travel

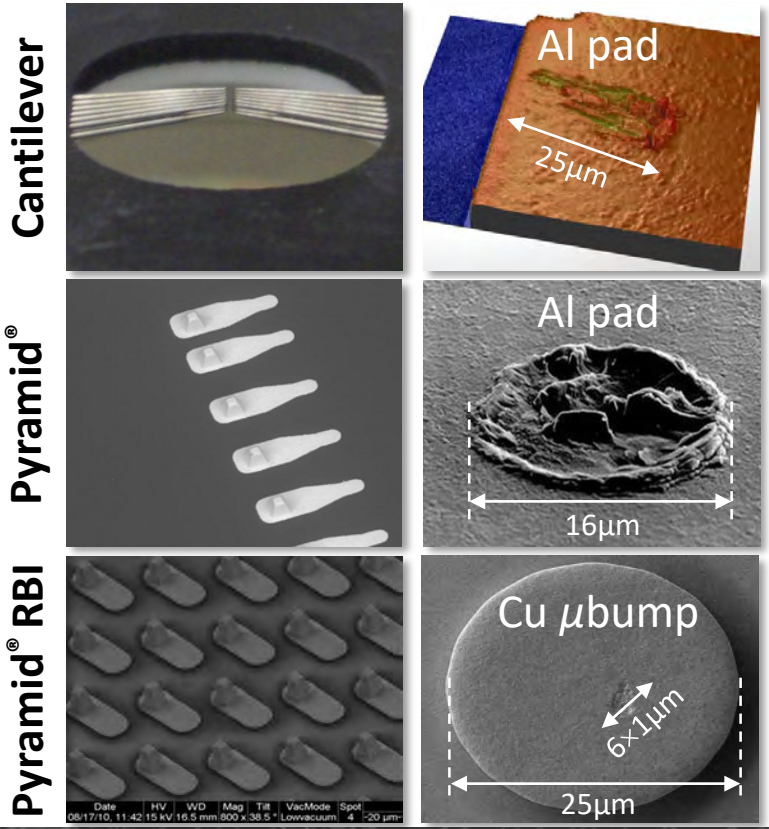


Probe Technologies and their Probe Marks



- **Cantilever probe card** (right)
  - Bulldozer trace ≥25µm
- **Vertical probe card** (left)
  - Smaller probe mark





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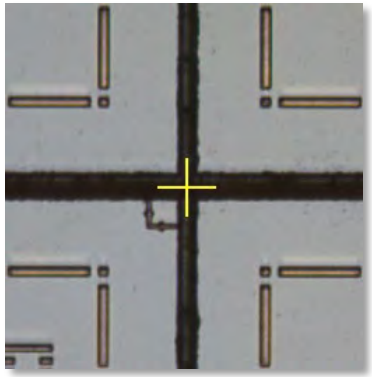
Singulated Die (Stacks) on Tape: Applications

- **Diced (and Thinned) Wafers**
  - Pre-bond test of D2D or D2W stacks
  - Test after dicing also covers dicing defects
- **Singulated D2W/W2W Stacks**
  - Mid-bond test of partial stacks
  - Post-bond test before packaging



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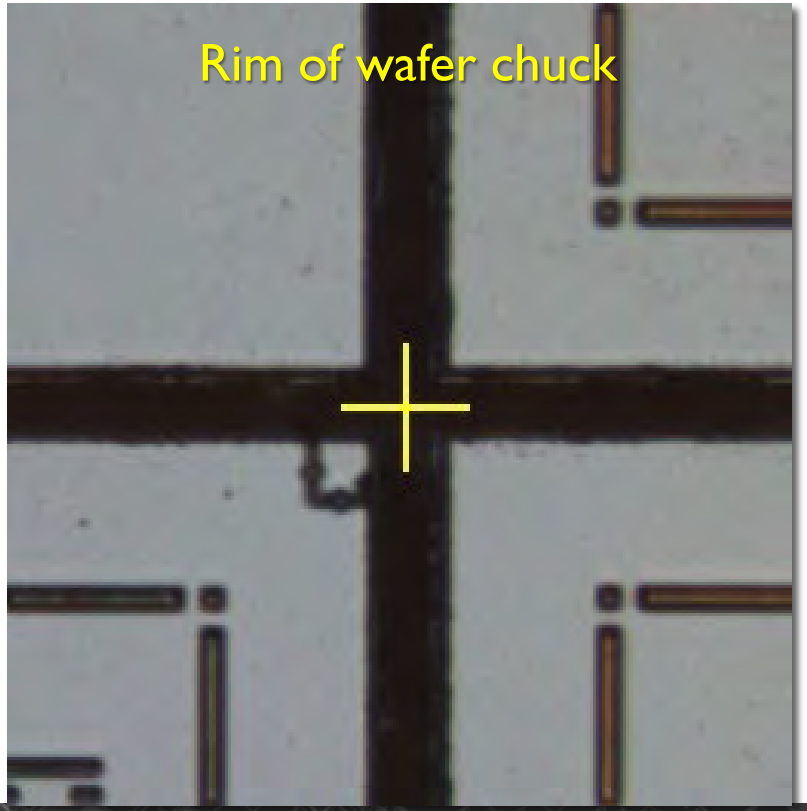

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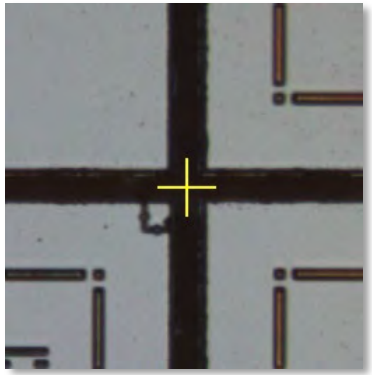
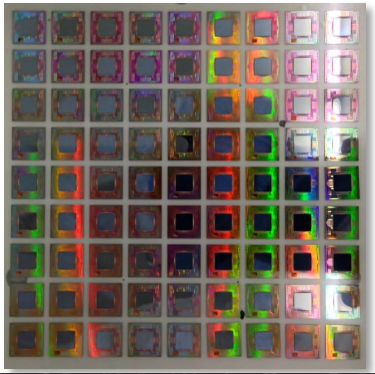
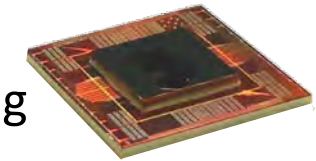
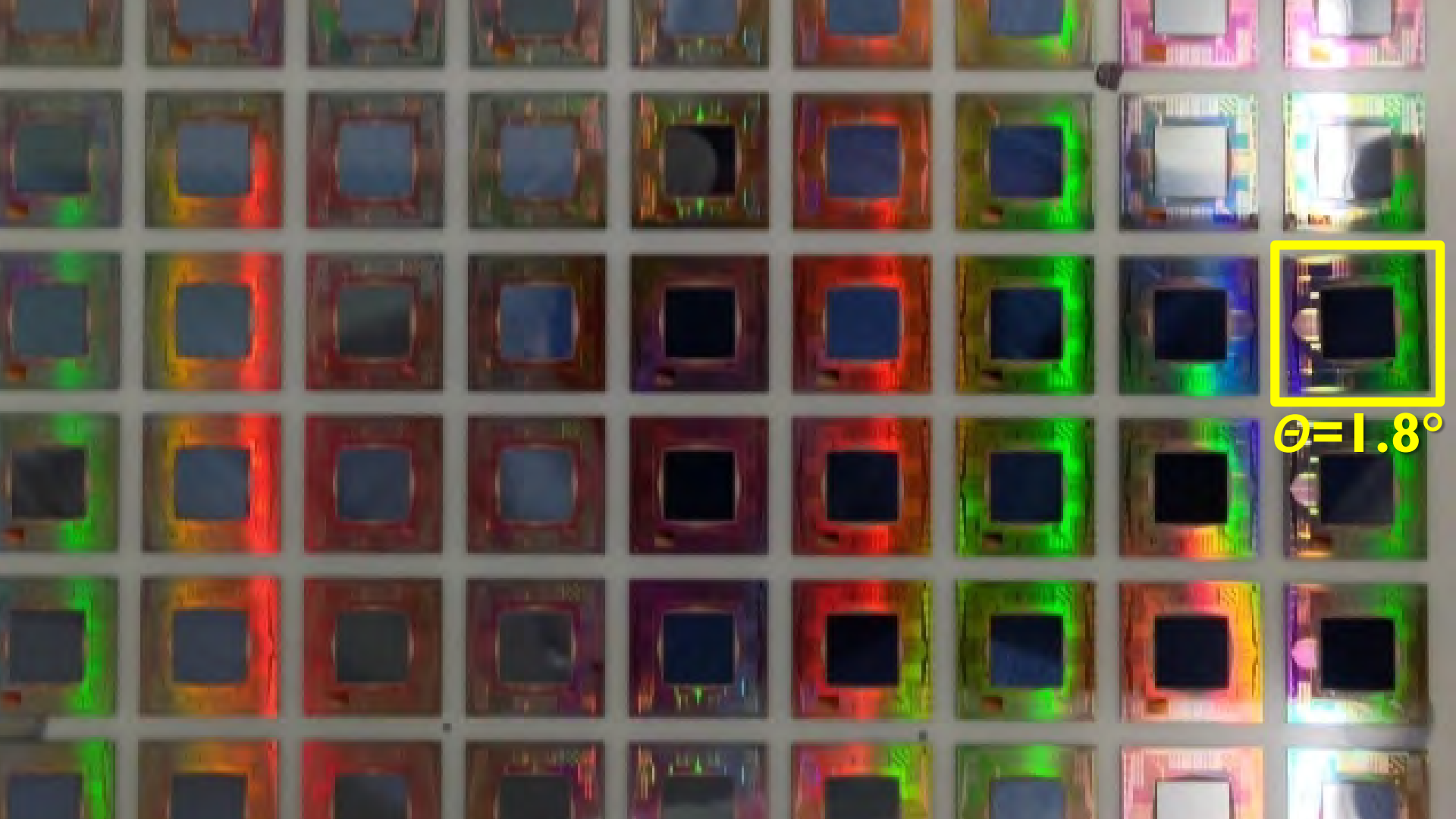
  - Mid-bond test of partial stacks
  - Post-bond test before packaging
- **Pick-n-Placed D2D Stacks**
  - PnP in matrix on carrier, e.g. tape frame
  - Allow automated testing through index stepping



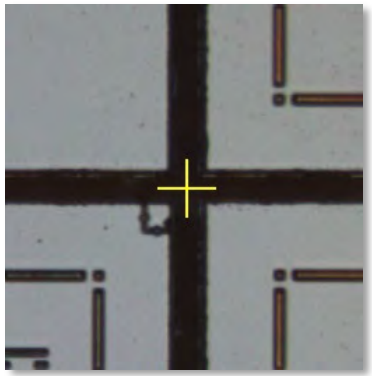


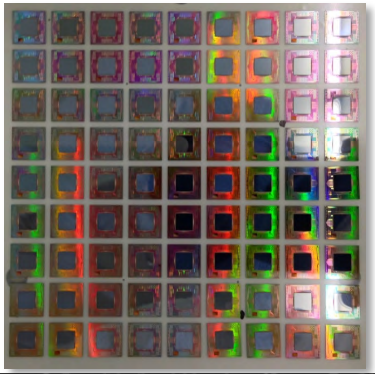


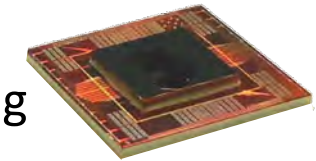

θ=1.8°

Singulated Die (Stacks) on Tape: Challenges

- **Diced (and Thinned) Wafers** ⇒ **Tape Stretch**
  - Pre-bond test of D2D or D2W stacks
  - Test after dicing also covers dicing defects
- **Singulated D2W/W2W Stacks** ⇒ **Tape Stretch**
  - Mid-bond test of partial stacks
  - Post-bond test before packaging
- **Pick-n-Placed D2D Stacks** ⇒ **PnP Inaccuracy**
  - PnP in matrix on carrier, e.g. tape frame
  - Allow automated testing through index stepping

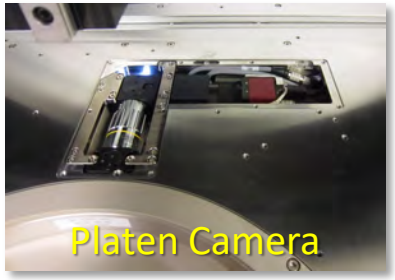




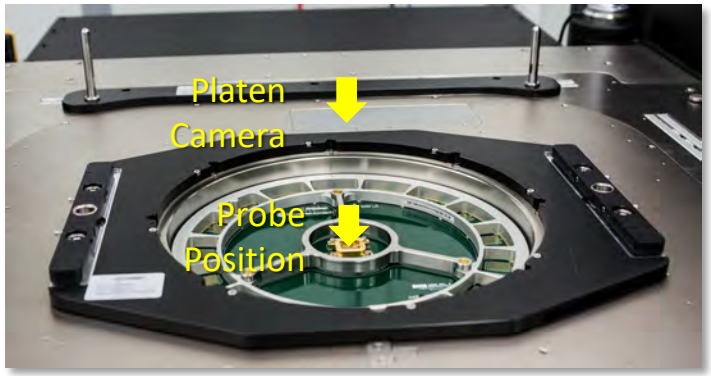


Automated Misalignment Correction by Prober

- **Probe Station's Job: Land Probes on Probe Targets**
  - Regular wafers: stepping with fixed index sizes
  - Singulated die (stacks) on tape: misalignments in *x*, *y*, *z*, and θ



- **FormFactor CM300 Prober Can Auto-Correct Misalignments**
  - *AlignChip*: per die correction of *x*, *y*, *z*, and θ
    - Requires alignment marks in FoV
    - θ compensation limited to ~2°
  - *PreMapWafer*: record all misalignments on single trip to Platen Camera; saves 13s/trip



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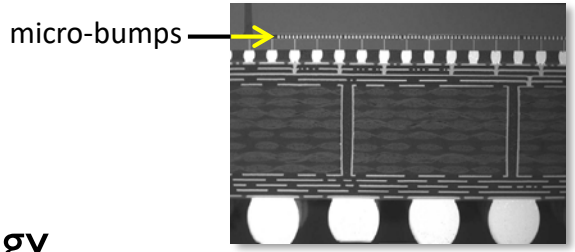
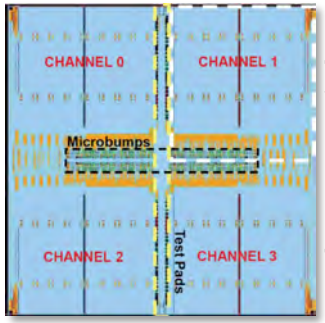
Direct Micro-Bump Probing



[Xilinx, 3D-TEST'12]

- **Functional interconnects** between 3D-stacked dies are implemented by large arrays of fine-pitch micro-bumps
- **Impossible** to probe with conventional probe technology
  - Cantilever probes : cannot form arbitrary arrays
    probe mark too large
  - Vertical probes : cannot handle the fine pitch

- **Options for pre-bond test**
  1. Skip pre-bond test: poor compound stack yield; higher cost
  2. Dedicated pre-bond probe pads: extra design, area, test time, post-bond load; and micro-bumps remain untested
  3. Use advanced probe technology to probe micro-bumps

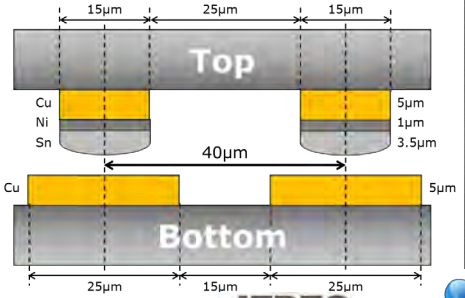


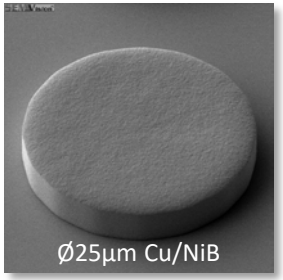
[Samsung, ISSCC'11]

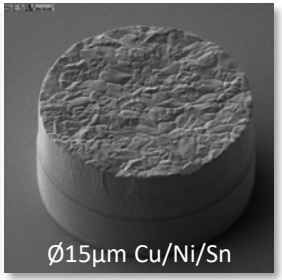
What Do We Want To Probe?

Micro-Bump Probe Targets

- imec's PoR @40µm pitch
- Today's advanced industry practice

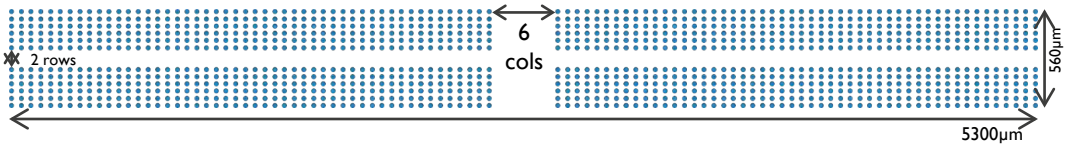


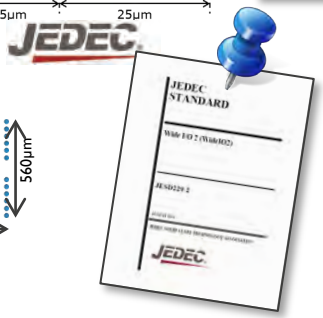




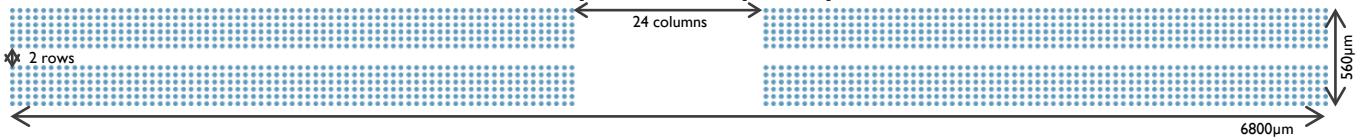
Wide-I/O Micro-Bump Arrays

- WIO1: 1,200 micro-bumps @50/40µm pitch

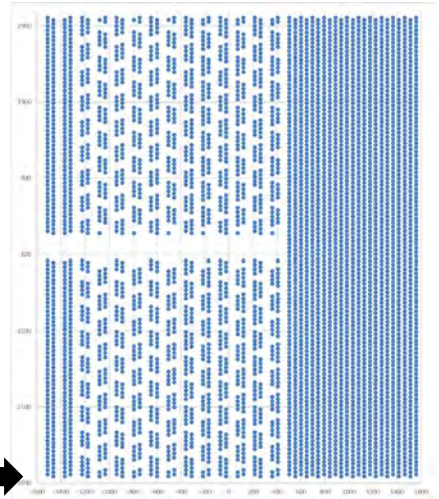




- WIO2: 1,752 micro-bumps @40µm pitch



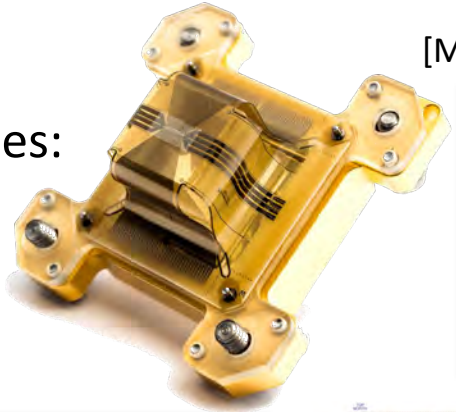
- HBM2: 4,258 micro-bumps @55µm pitch

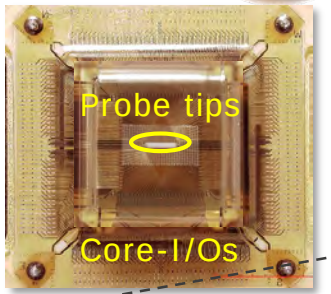


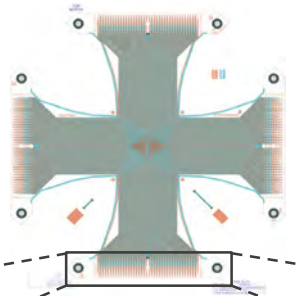
FormFactor Pyramid® Probes RBI

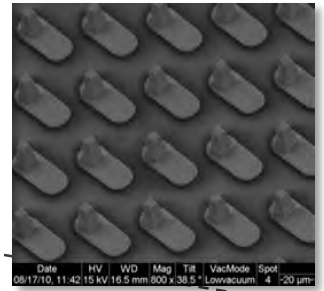
- **Modular**: card + core + tip coupon
- **Core**: frame with two thin-film membranes: (1) tip layer; (2) routing layer
  - Tip coupon is replaceable
- **Vertical MEMS-Type Probes**
  - Tips: 6×6µm², 6×1µm² probe mark
  - Full-arrays down to 20µm pitch
  - Litho-defined: perfect pitch (but membrane can stretch)
- **R&D**, not (yet) a catalogue product
- **@imec**: WIO1 and WIO2

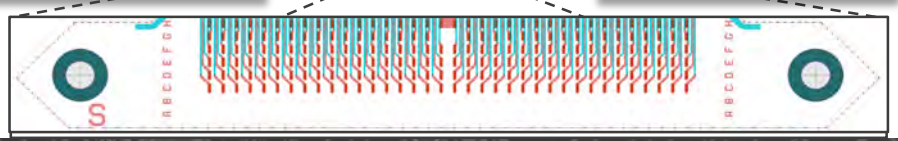
[Marinissen et al. – ITC Asia'17]











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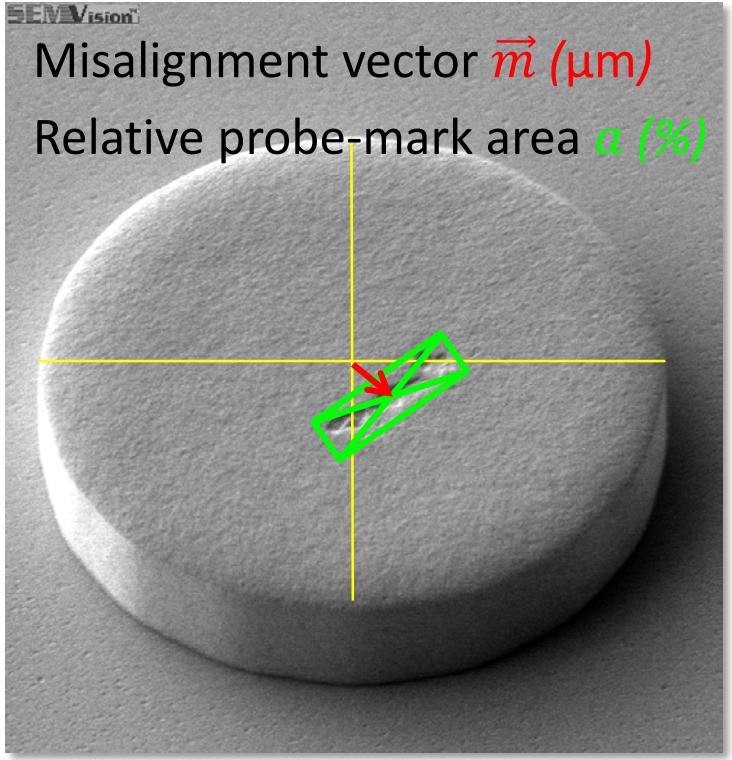
Probe-To-Pad Alignment (PTPA) Accuracy

PTPA Accuracy Assessment Procedure

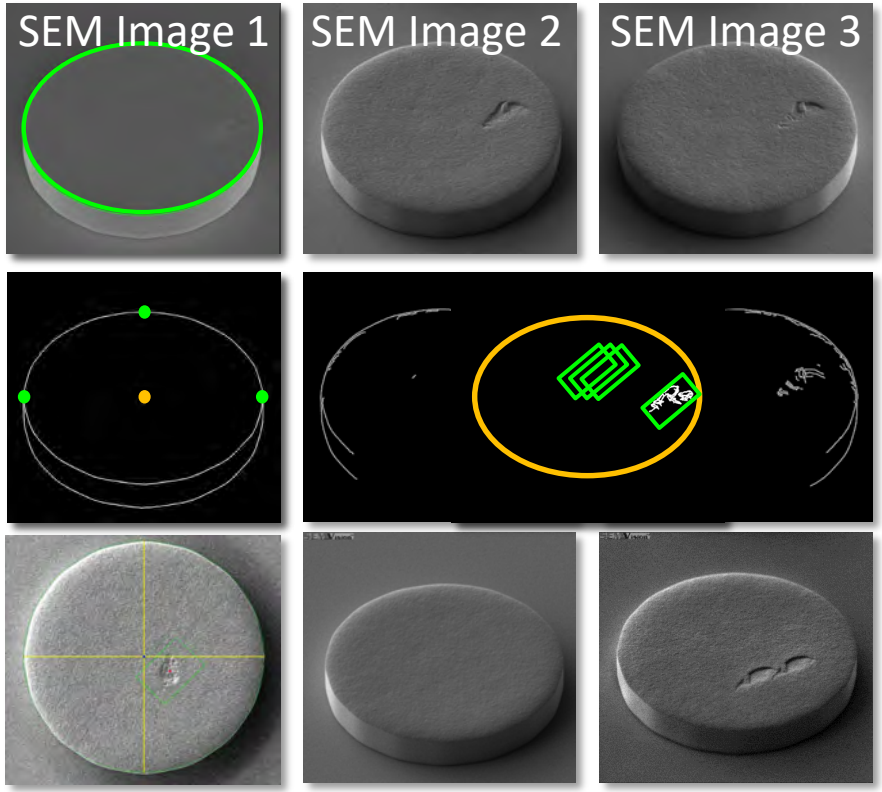
1. Train probe card on station
   - Define home die; main alignment BL
2. Probe all micro-bump arrays on wafer
3. SEM images of corners of probed arrays
4. Measure for each micro-bump:
   - Bump : center (x_{mb}, y_{mb}), area a_{mb}
   - Mark : center (x_{pm}, y_{pm}), area a_{pm}
5. Calculate misalignment $\vec{m} = (x_{pm} - x_{mb}, y_{pm} - y_{mb})$ and relative probe-mark area $a = a_{pm}/a_{mb}$



Automatic Probe-Mark Analysis

[Rong et al. – SWTW'18]

- **One SEM Shot: Three Images**
  - Image sharpening
  - Edge detection
- **Micro-Bump Contour**: Image 1
  $\Rightarrow$ center + area
- **Probe Mark Contour**: Images 2+3
  $\Rightarrow$ center + area
- **Software Tool Also Handles**
  - Top-view vs. tilted view
  - No or multiple probe marks



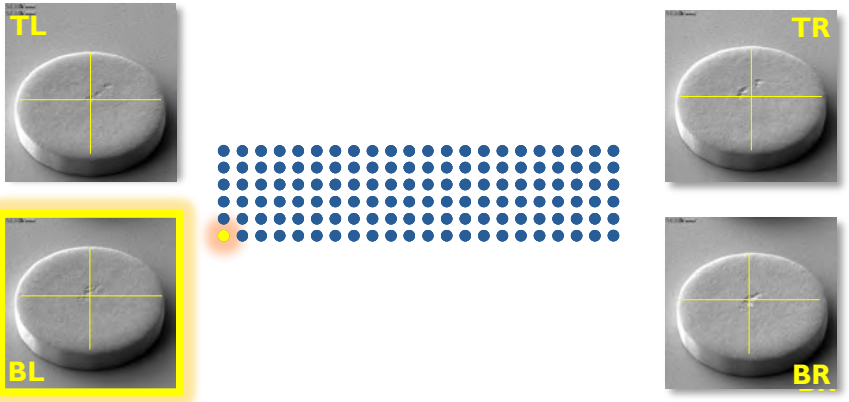
Separating PTPA Accuracy Contributions: Station

1. Probe-Station Accuracy

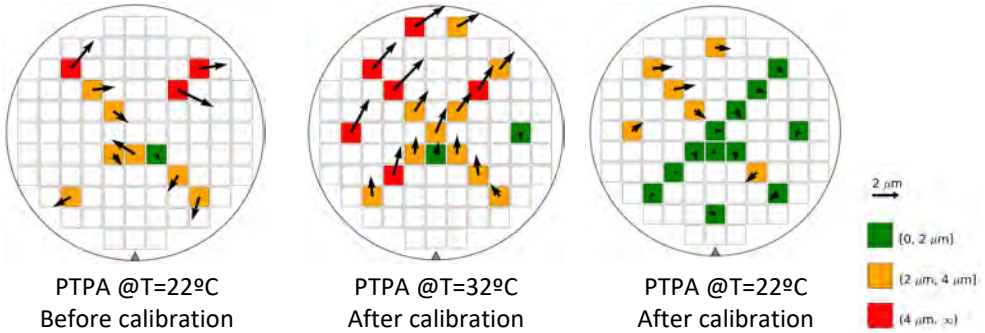
- Misalignment of BL corner per die ***d***:

$$\vec{m}_{station}(d) = \vec{m}(BL_d)$$

- Chuck-position dependent
  → Alignment error wafer map



- **Regular Calibration** of the 'Compensation Matrix' is required
  - Software compensation for small mechanical misalignments between (1) probe and (2) platen positions
- **Thermal Control** to avoid radial wafer expansion



PTPA @T=22ºC
Before calibration

PTPA @T=32ºC
After calibration

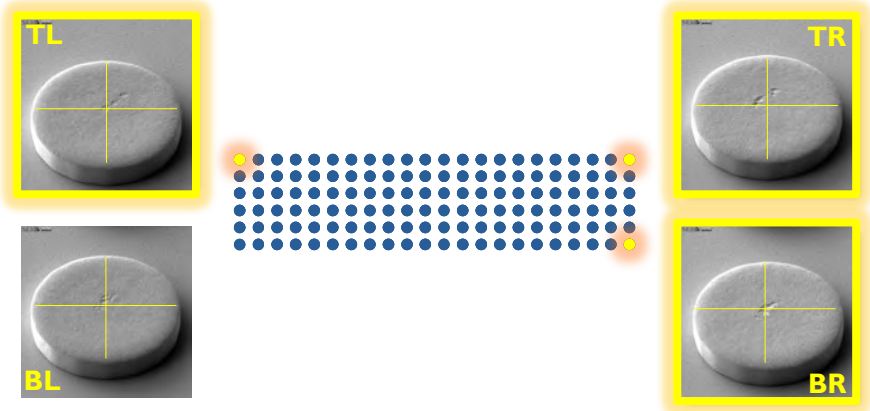
PTPA @T=22ºC
After calibration

Separating PTPA Accuracy Contributions: Card

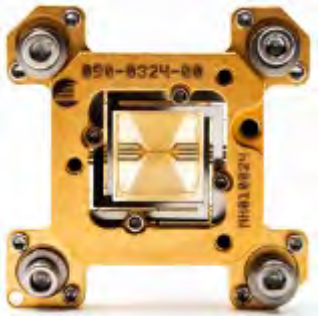
2. Probe-Card Accuracy

- Errors on other corners due to card
- Translate misalignments for die ***d***, corner $\boldsymbol{c} \in \{BL, BR, TR, TL\}$:

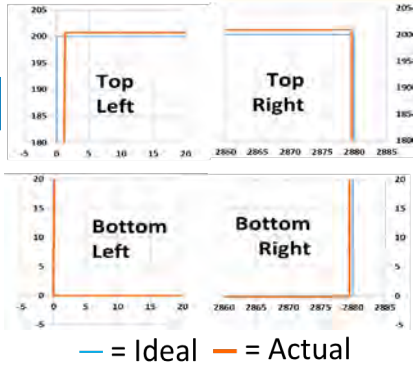
$$\vec{m}_{card}(c) = \vec{m}(c_d) - \vec{m}(BL_d)$$



WIO2-1Bank



Corner *c*	Ideal (µm) (x_{mb}, y_{mb})	Actual (µm) (x_{pm}, y_{pm})	Error (µm) *m(c)*	Relative Error *x*	Relative Error *y*
BL	(0, 0)	(0.00, 0.00)	(0.00, 0.00)	0.00%	0.00%
BR	(2880, 0)	(2879.47, -0.12)	(-0.53, -0.12)	-0.02%	+0.06%
TR	(2880, 200)	(2879.61, 200.88)	(-0.39, 0.88)	-0.01%	+0.44%
TL	(0, 200)	(1.33, 200.71)	(1.33, 0.71)	-0.05%	+0.35%



Presentation Outline

1. Introduction
2. Probing on Large Tape Frames
3. Probing on Ultra-Thin Wafers on Tape
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5. Probing Dense Arrays of Micro-Bumps
6. PTPA Accuracy Assessment
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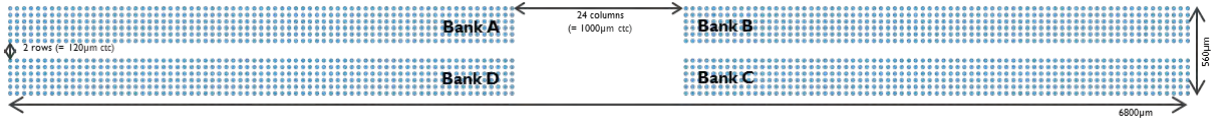
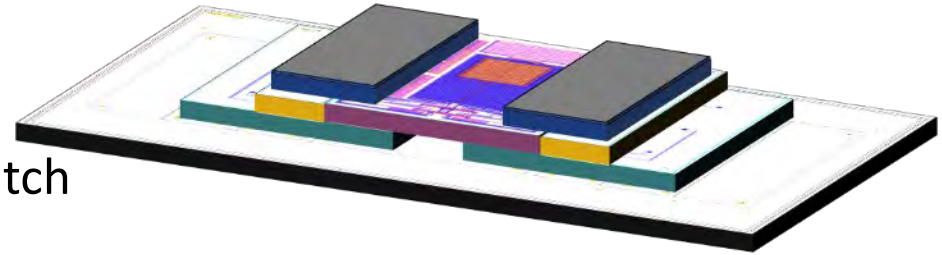
8. Conclusion

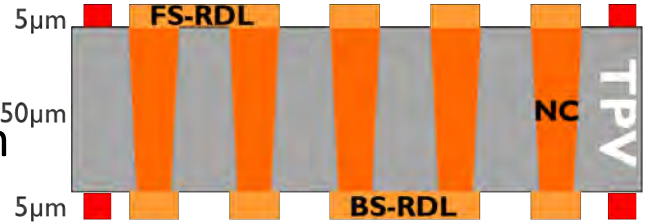
Example: TPV Die



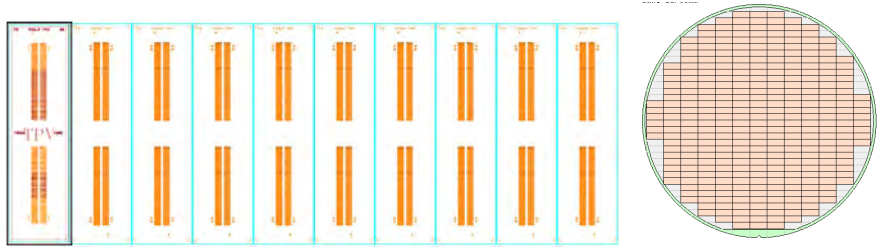
- **Design**: 2.0×8.0mm²
  - Dense low-cost vertical interconnect
  - Wide-I/O2: 1,752× bumps @40µm pitch



- **Technology**:
  - TSVs: Cu, ∅5µm×50µm high
  - Front-side RDL: } Cu, micro-bumps ∅25µm×5µm
  - Back-side RDL: } Cu, interconnects 5µm×5µm



- **Manufacturing at imec**
  - Reticle with 10 dies
  - Ø300mm wafers, 3260 dies



TPV Pre-Bond Test Involves All Challenges

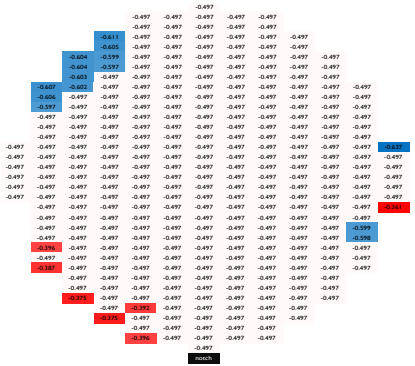
- **Probing Challenges Addressed in Conjunction**

1. Probing on large tape frames	SEMI Std G74-0669
2. Probing on ultra-thin wafers on tape	50µm thickness (due to TSV)
3. Probing dense arrays of micro-bumps	WIO2; 1,752 bumps @40µm
4. PTPA accuracy assessment	Used automatic analysis software
5. Probing singulated dies on tape	3,260 diced dies, ∅300mm wafer

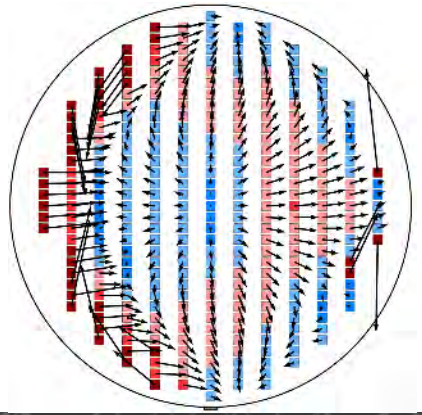
- **Reported Results**
  - Automated misalignment corrections in θ and x, y
  - Probe marks and electrical results

Automated Misalignment Correction by Prober

- **Rotation θ**
  - Most die: θ = -0.497° (manual loading)
  - 6.4% outliers: θ∈[-0.637°...-0.361°]
- **Translation *x*,*y***
  - Large deviations (>500µm) from index position
    - Most dies follow stretch forces of dicing tape
    - Same outlier dies require large translations in opposite directions
- **Significant Chuck Travel Time Reduction**
  - *'PreMapWafer'* saved 3260× 13s ≈ 700 min.

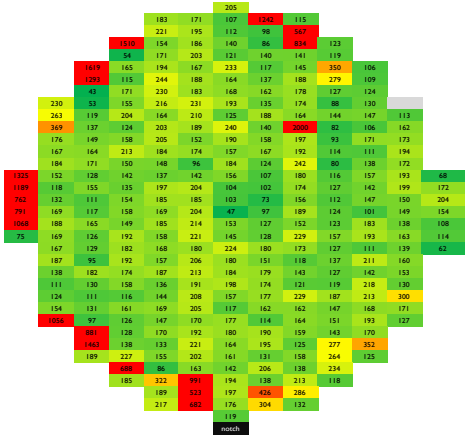


	Misalignment	
	Avg.	Max.
θ	-0.497º	-0.637º
x	116µm	351µm
y	232µm	576µm

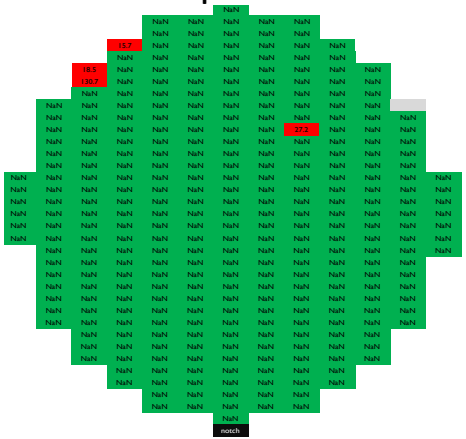


Electrical Results and Probe Marks

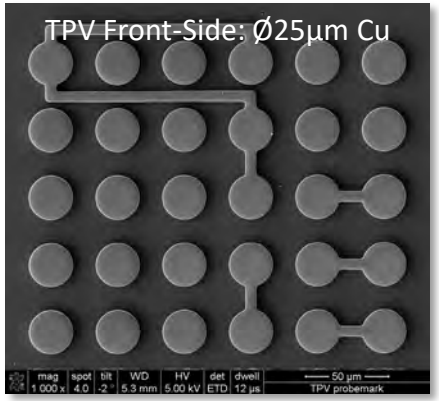
Wafer Map:
FS-Short Test on Bank *A*

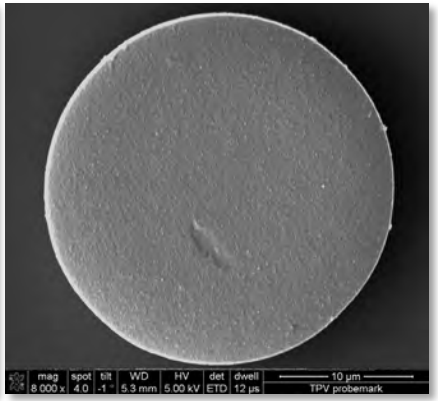


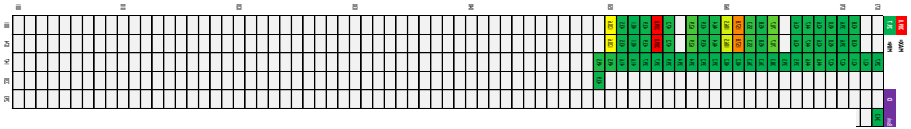
Wafer Map:
NC-Open Tests

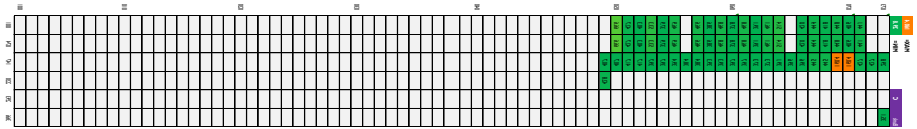


Probe Marks:
Arbitrary (probed) array

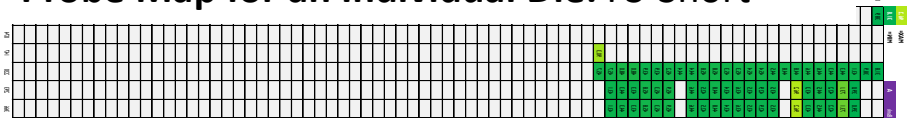


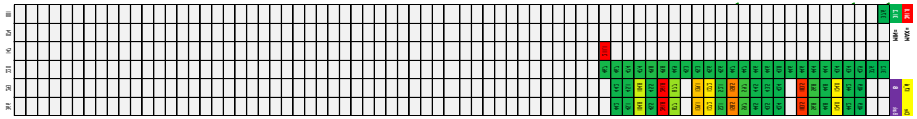






Probe Map for an Individual Die: FS-Short





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A ‘Toolbox’ for Probing Challenges in (3D-)Test

Challenges	Solutions
1. Probing on large tape frames	Adapted probe station
2. Probing on ultra-thin wafers on tape	Low-force probe cards
3. Probing dense arrays of micro-bumps	Advanced probe cards + stations
4. PTPA accuracy assessment	Automatic analysis software
5. Probing singulated die (stacks) on tape	Auto-correction by prober software

- These solutions can be used stand-alone or in conjunction with each other
  - TPV case study demonstrated successful results with all solutions together
- Contribution to productization of multi-die stacks
- Full paper: Marinissen et al. – ITC’18 – DOI: 10.1109/TEST.2018.8624731

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