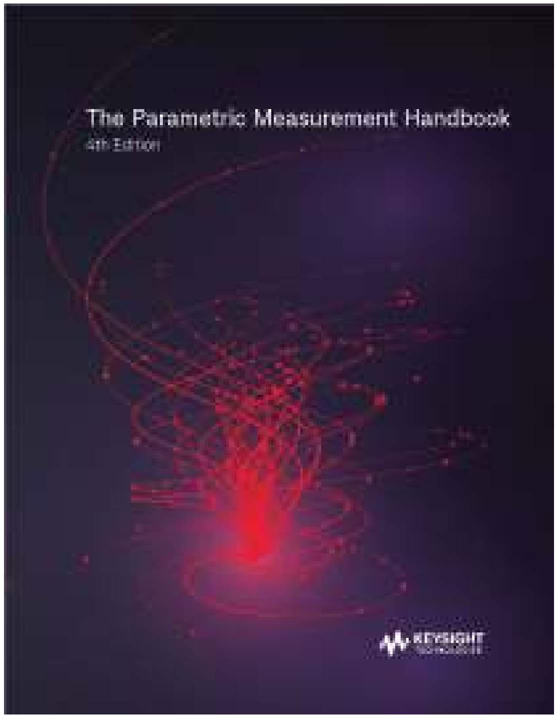
# Techniques for the Efficient Characterization of Wide Bandgap Power Devices

**Joshua Sarris – Application Engineer**

**Keysight Technologies**

# Before We Begin


The Parametric Measurement Handbook
4th Edition
KEYSIGHT

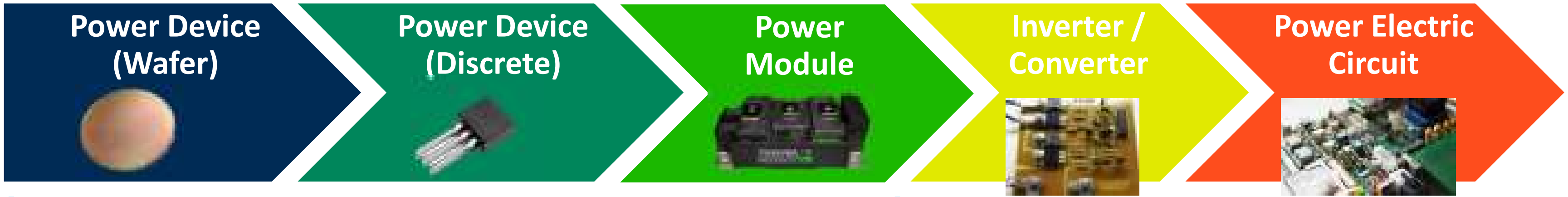
Everything covered in this presentation is explained in greater detail in the latest version (4th edition) of our 276-page Parametric Measurement Handbook.

You can download a copy for free at:
https://connectlp.keysight.com/ParametricHandbook

# Measurement Equipment Used

**B1506A**
- 3kV, 20A/500A/1500A models
- Automated and easy to use operation
- Quick datasheet validation
- Power loss calculation using I-V, C-V, Rg, Qg
- Automated thermal test -50°C to +250°C

For power electronics engineers using power devices in their products



**Power Device (Wafer)**

**Power Device (Discrete)**

**Power Module**

**Inverter / Converter**

**Power Electric Circuit**

For power semiconductor manufacturers

**B1505A**
- Flexible and scaleable configuration
- Covers both on-wafer and packaged devices
- Microvolts to 10kV
- Picoamps to 1500A
- Supports familiar EasyEXPERT software

# High Power Wafer Probing Example

Tesla Probe Station with B1505A

High Power Probes

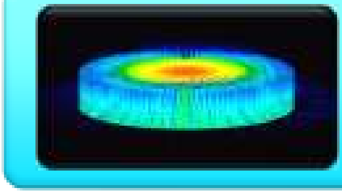
# Agenda for Today

1. *Why Use Wide Band Gap Devices?*
2. *Calculating Power Loss in Power Semiconductor Devices*
3. *Measuring Power Device Capacitance*
4. *Measuring Power Gate Charge*
5. *Power Analysis for Energy Conversion Devices*

# Why Use Wide Bandgap Semiconductors?

## Improved Conversion Efficiency

- Reduced losses (switching and conduction)
- Higher voltages & currents
- Higher frequency



## Smaller & Lighter Cooling Systems

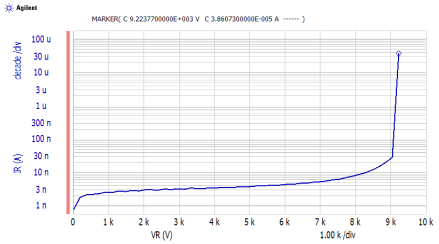
- Higher operating temperatures

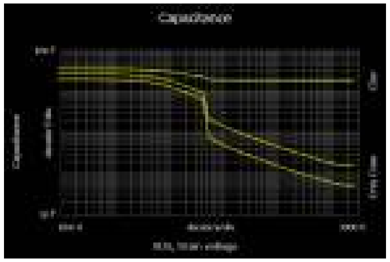
## Reduced Volume and Weight

- Higher Integration

# WBG Semiconductor Evaluation Challenges

- ◆ Higher current force/measurement (>100 A)
- ◆ Higher voltage force/measurement (up to 10 kV)
- ◆ Accurate low on-resistance ($R_{on}$) measurement (sub-mΩ)
- ◆ Capacitance measurements at high voltage (up to 3 kV)
- ◆ Gate charge measurement at high current & voltage (>100 A & >1 kV)
- ◆ Quantitative GaN current collapse effect characterization





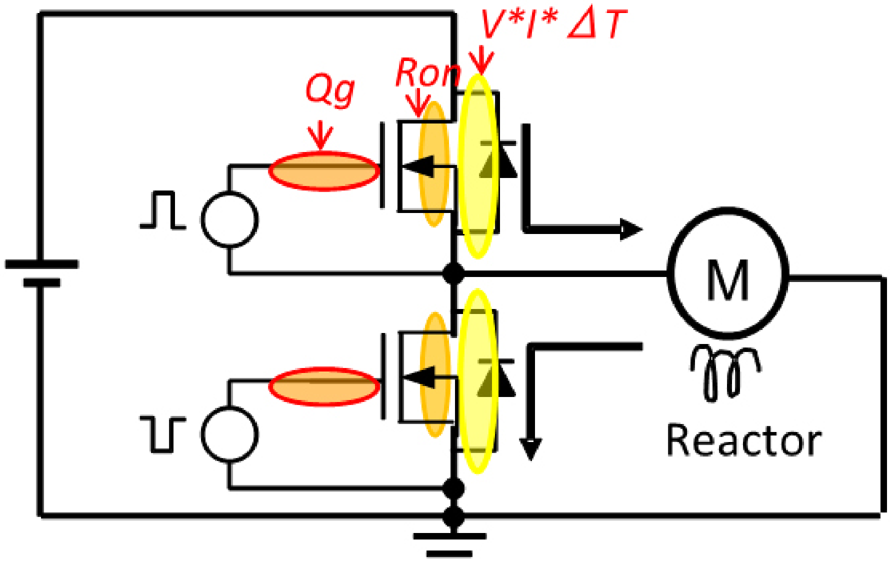
| | **SiC device** | **GaN device (on Silicon)** |
|---|---|---|
| Power range | Several 100’s kW | Few kW |
| Max Vb | 10 kV | Few kV |
| $R_{on}$ (per area) | <10 mΩ/cm$^2$ | 1 mΩ/cm$^2$ |

# Agenda for Today

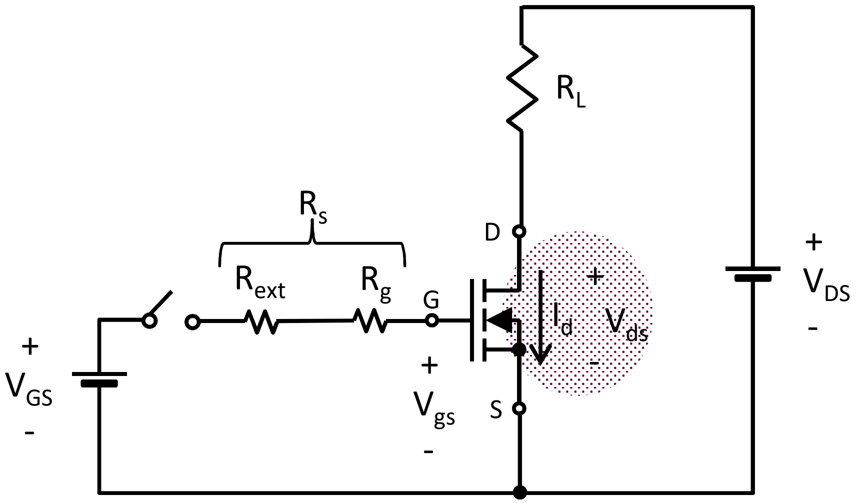
1. *Why Use Wide Band Gap Devices?*
2. *Calculating Power Loss in Power Semiconductor Devices*
3. *Measuring Power Device Capacitance*
4. *Measuring Power Gate Charge*
5. *Power Analysis for Energy Conversion Devices*

# The Components of Power Loss

| Total Loss = | Conduction Loss + | Switching Loss + | Driving Loss |
|---|---|---|---|
| **Key Parameters:** | $R_{on}$ | $R_g, C_{rss}, C_{oss}$ | $Q_g$ |



# Conduction Loss – Ohmic (IR) Power Consumption

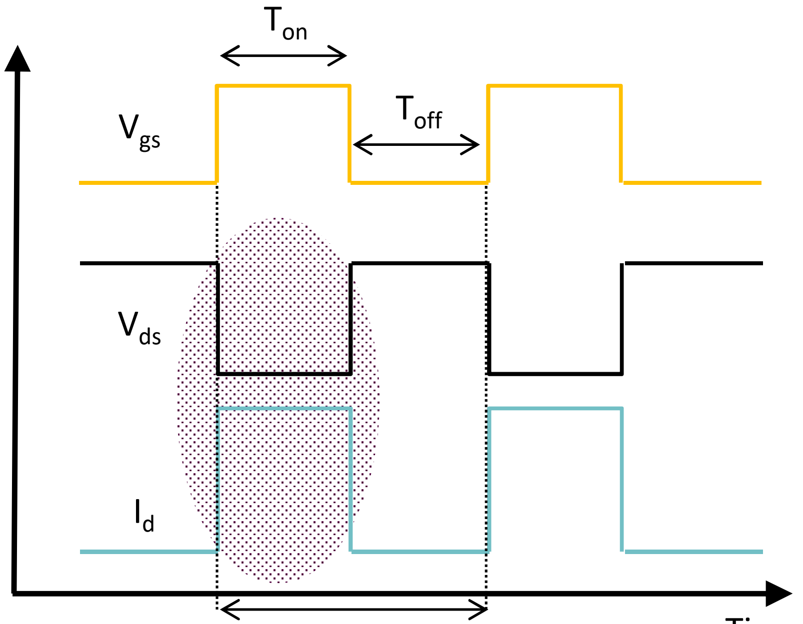


**For MOSFETs:**

$$P_{cond} = Id \times Vds \times Duty\ Ratio$$
$$= Id^2 \times Rds(on) \times Duty\ Ratio$$

**For IGBTs:**

$$P_{cond} = Ic \times Vce(sat) \times Duty\ Ratio$$

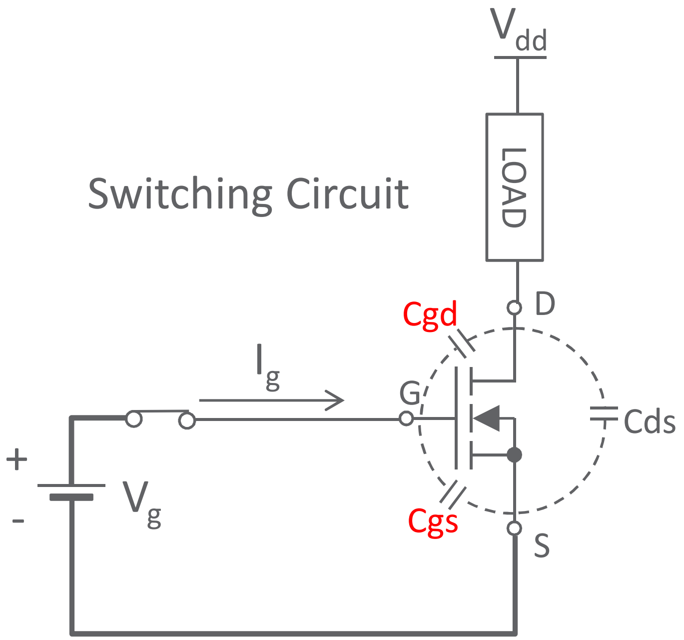


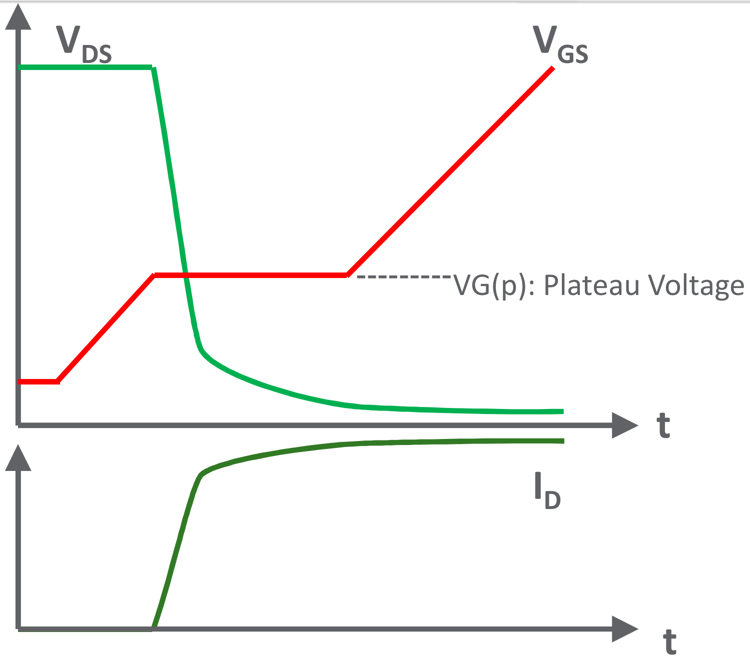
Period = 1 / Frequency

Duty Cycle = Ton / Period

# What is Gate Charge – Qg?

Switching Circuit





- Qg is the charge necessary to turn on or turn off a device
- Qg is a key parameter to estimate device switching loss
- Q = CV = $\int Ig$ dt

# Why is Qg Important?

- **One of the key design parameters for gate drive circuits**
  - Output voltage and current capability
  - Qg is listed in virtually all power MOSFET and IGBT datasheets
- **Switching time parameters can be estimated from the Qg curve**
  - More accurate simulation is possible as compared to using only capacitance parameters
  - Switching time parameters can be used to estimate the overall switching loss
- **Important component of overall WBG power loss**
  - For WBG devices power loss is determined by switching and driving loss

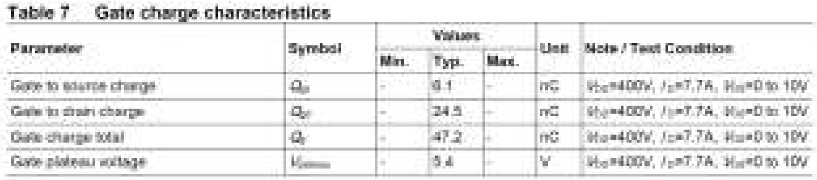
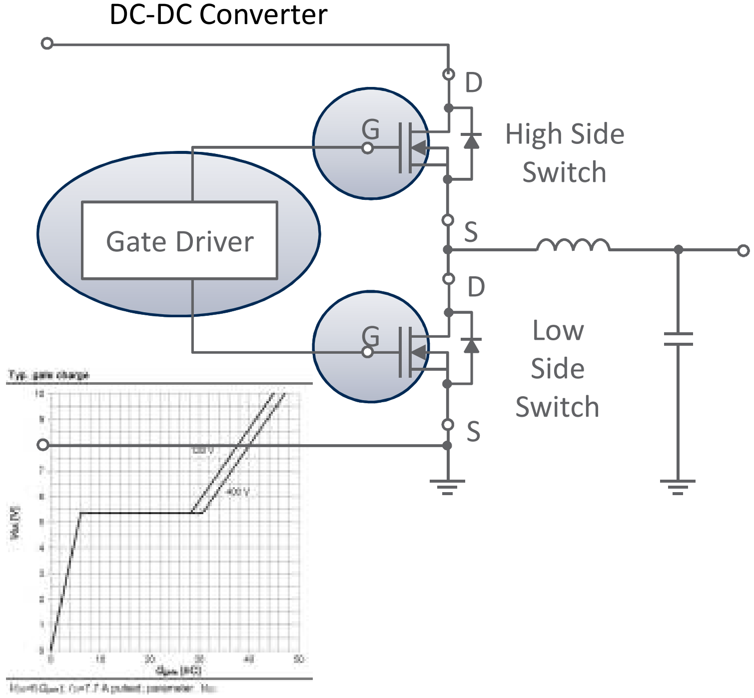


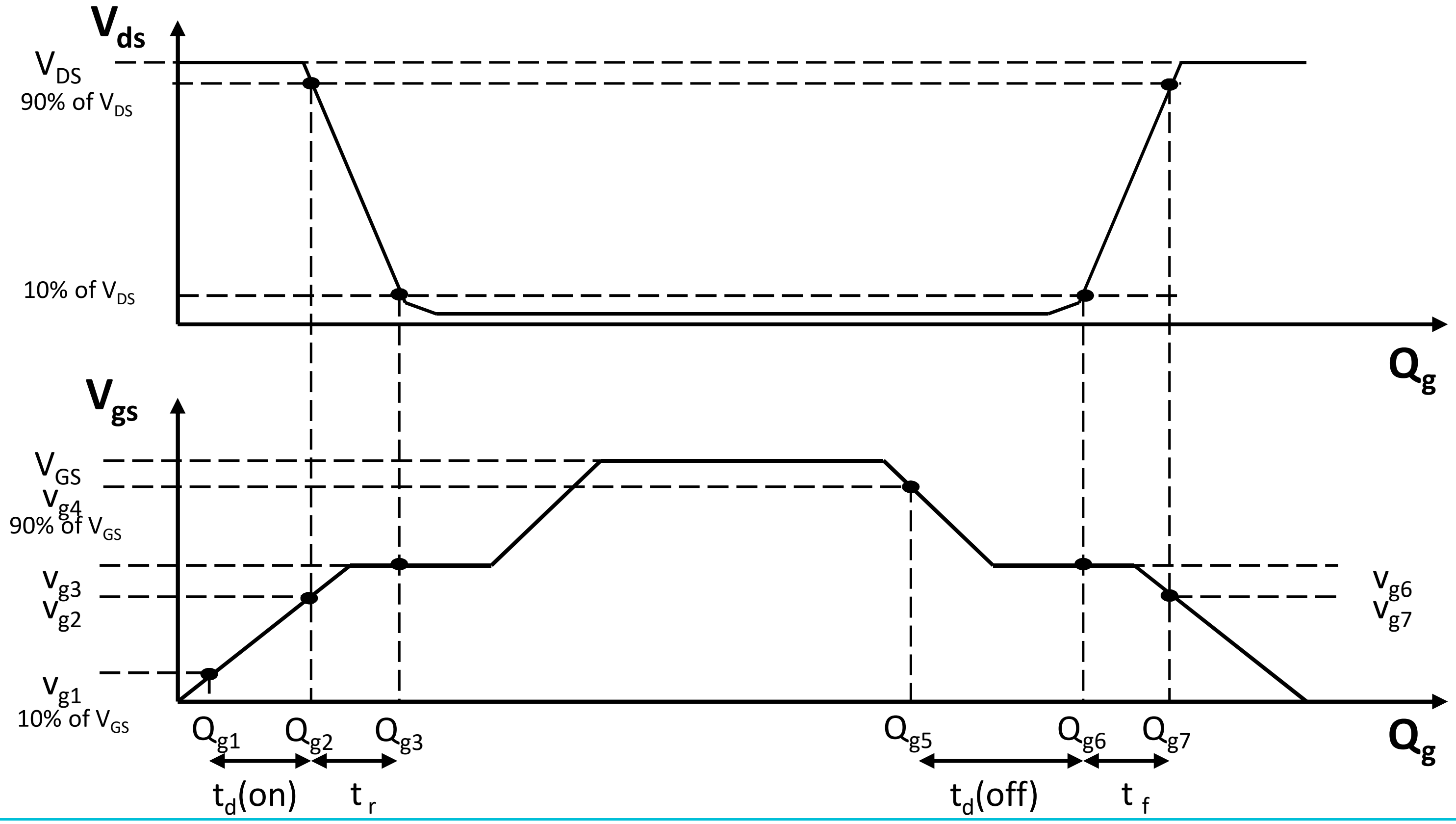
Table 7 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 8.1 | - | nC | $V_{DD}$=400V, $I_D$=7.7A, $V_{GS}$=0 to 10V |
| Gate to drain charge | $Q_{gd}$ | - | 24.5 | - | nC | $V_{DD}$=400V, $I_D$=7.7A, $V_{GS}$=0 to 10V |
| Gate charge total | $Q_g$ | - | 47.2 | - | nC | $V_{DD}$=400V, $I_D$=7.7A, $V_{GS}$=0 to 10V |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}$=400V, $I_D$=7.7A, $V_{GS}$=0 to 10V |



$V_{GS}$=f($Q_{gate}$); $I_D$=7.7 A pulsed; parameter: $V_{DD}$

# Graphs Relating Vds, Vgs and Qg

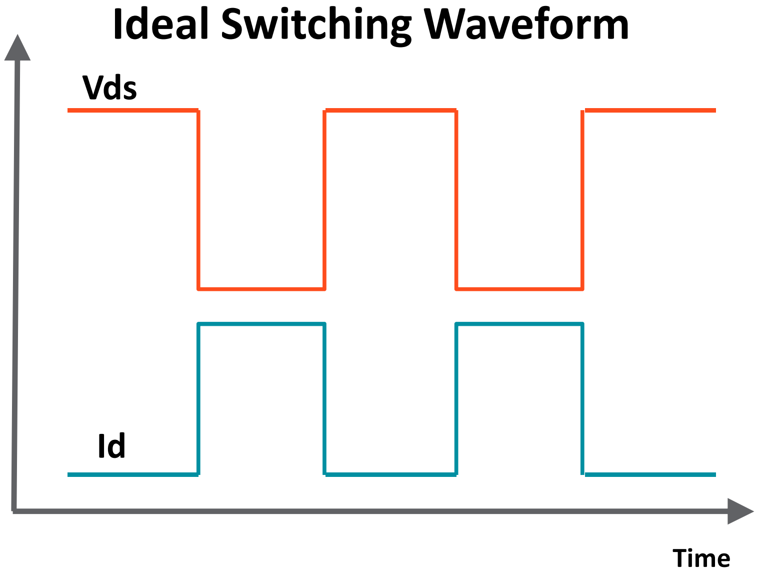


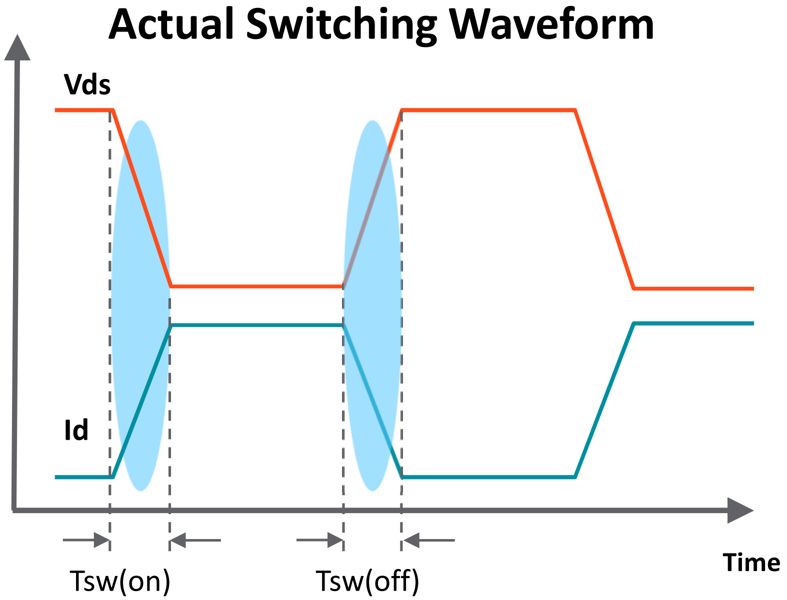
# Summarized Switching Time Equations

| | |
|---|---|
| Turn On Delay Time<br>(10% of $V_{GS}$ to 90% of $V_{DS}$) | $t_d(on) = \left(\frac{Q_{g2} - Q_{g1}}{V_{g2} - V_{g1}}\right) * R_s * ln\left\{\frac{V_{GS} - V_{g1}}{V_{GS} - V_{g2}}\right\}$ |
| Rise Time<br>(90% of $V_{DS}$ to 10% of $V_{DS}$) | $t_r = \left(\frac{Q_{g3} - Q_{g2}}{V_{g3} - V_{g2}}\right) * R_s * ln\left\{\frac{V_{GS} - V_{g2}}{V_{GS} - V_{g3}}\right\}$ |
| Turn Off Delay Time<br>(90% of $V_{GS}$ to 10% of $V_{DS}$) | $t_d(off) = \left(\frac{Q_{g6} - Q_{g5}}{V_{g6} - V_{g5}}\right) * R_s * ln\left\{\frac{V_{g6}}{V_{g5}}\right\}$ |
| Fall Time<br>(10% of $V_D$ to 90% of $V_{DS}$) | $t_f = \left(\frac{Q_{g7} - Q_{g6}}{V_{g7} - V_{g6}}\right) * R_s * ln\left\{\frac{V_{g7}}{V_{g6}}\right\}$ |

See Parametric Measurement Handbook for detailed equation derivations.

# Switching Loss





**Switching time = 0 s** ⇨ **Switching Loss = 0 W** **Switching time > 0 s** ⇨ **Switching Loss > 0 W**

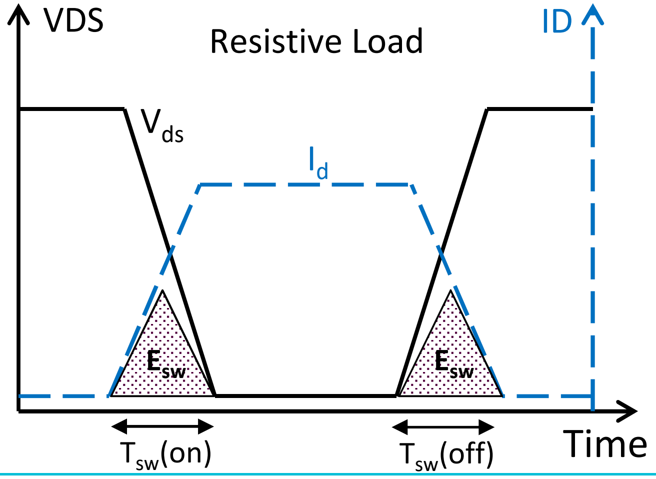
➔ Need to Know the Switching Time!

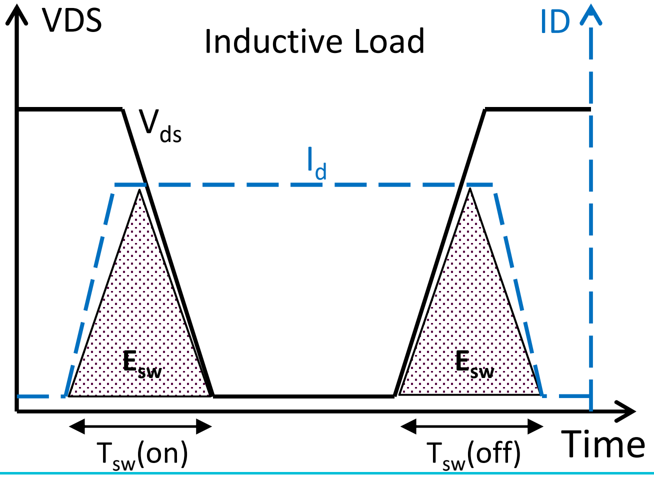
# Summarized Switching Loss Equations

$$T_{sw}\ (on) = \frac{Q_{sw}}{i_g} = R_s * \frac{Q_{sw}}{V_{GS} - V_{gp}} \qquad T_{sw}\ (off) = \frac{Q_{sw}}{i_g} = R_s * \frac{Q_{sw}}{V_{gp}}$$

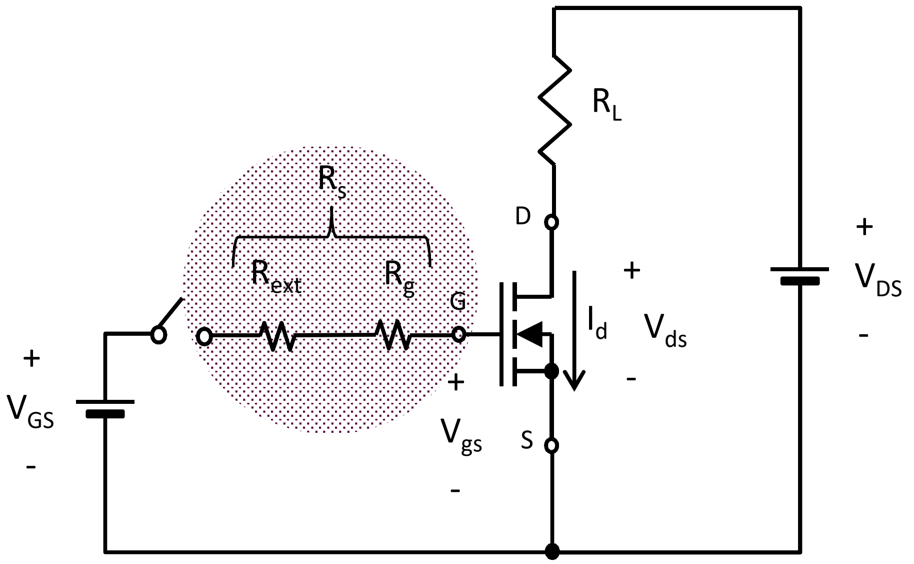
$$P_{sw}(resistive) = \left(\frac{1}{6}\right) * V_{DS} * I_D * (T_{sw}(on) + T_{sw}(off)) * f$$

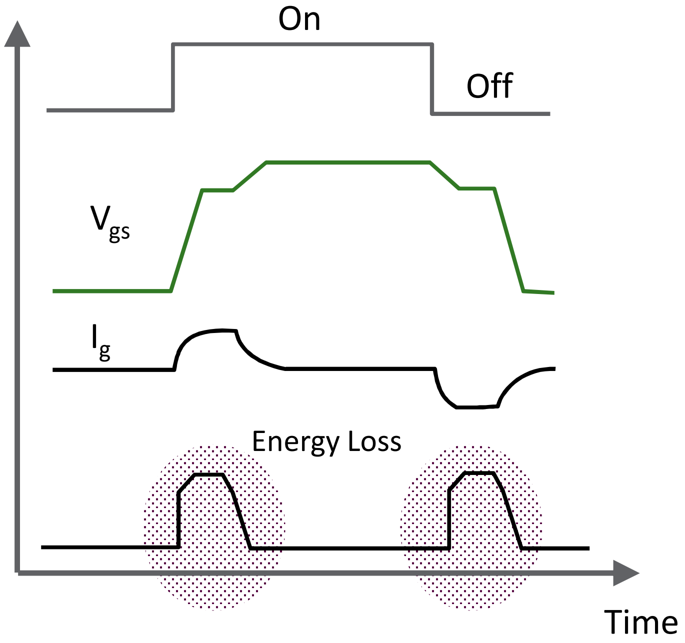
$$P_{sw}(inductive) = \left(\frac{1}{2}\right) * V_{DS} * I_D * (T_{sw}(on) + T_{sw}(off)) * f$$





# Driving Loss





$$E = \frac{1}{2}CV^2 = \frac{1}{2}QV$$

$$P_d(on) = \frac{1}{2}Qg(on) \times Vgs \times Frequency$$

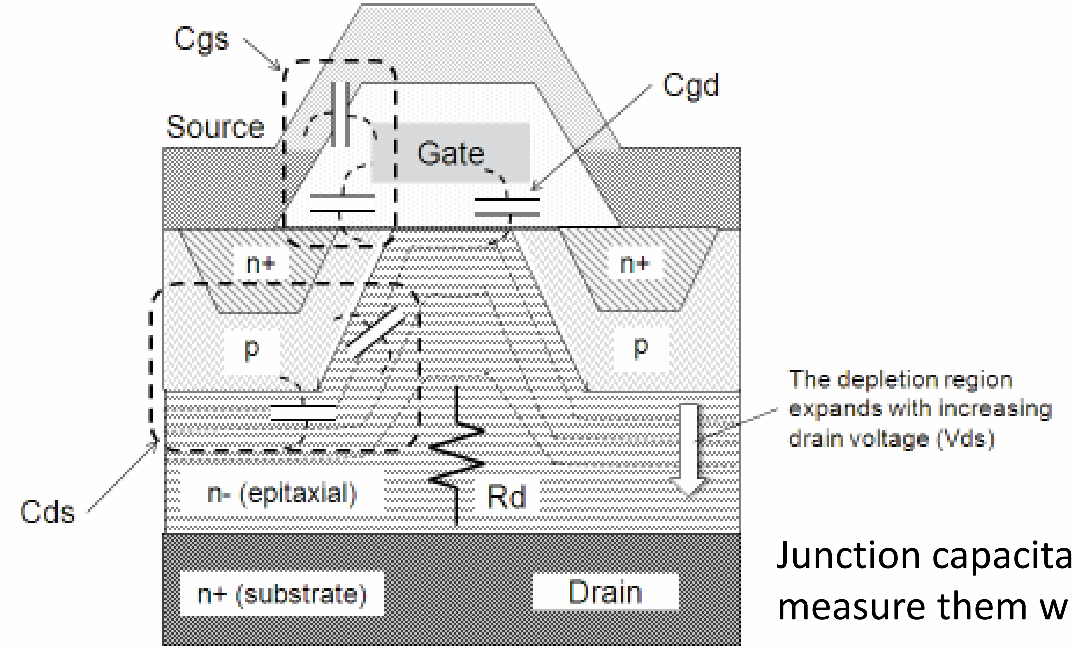
$$Qg(on) = Qg(off)$$

$$P_d = Qg \times Vgs \times Frequency$$

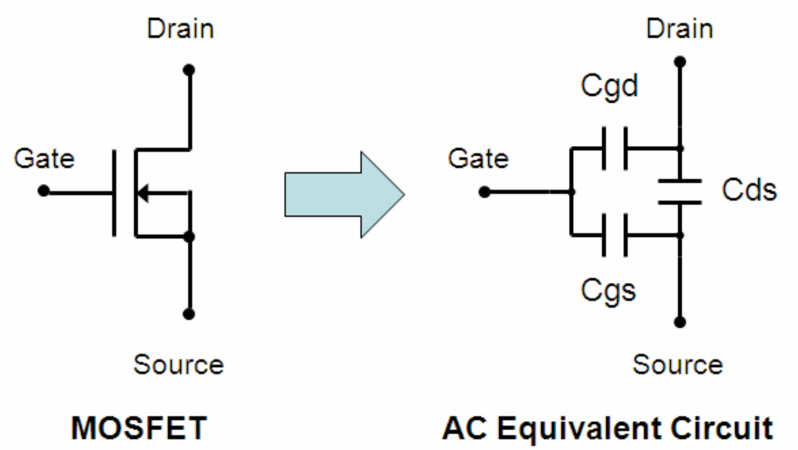
# Agenda for Today

1. *Why Use Wide Band Gap Devices?*
2. *Calculating Power Loss in Power Semiconductor Devices*
3. *Measuring Power Device Capacitance*
4. *Measuring Power Gate Charge*
5. *Power Analysis for Energy Conversion Devices*

# Power MOSFET Capacitance Measurement



The depletion region expands with increasing drain voltage (Vds)

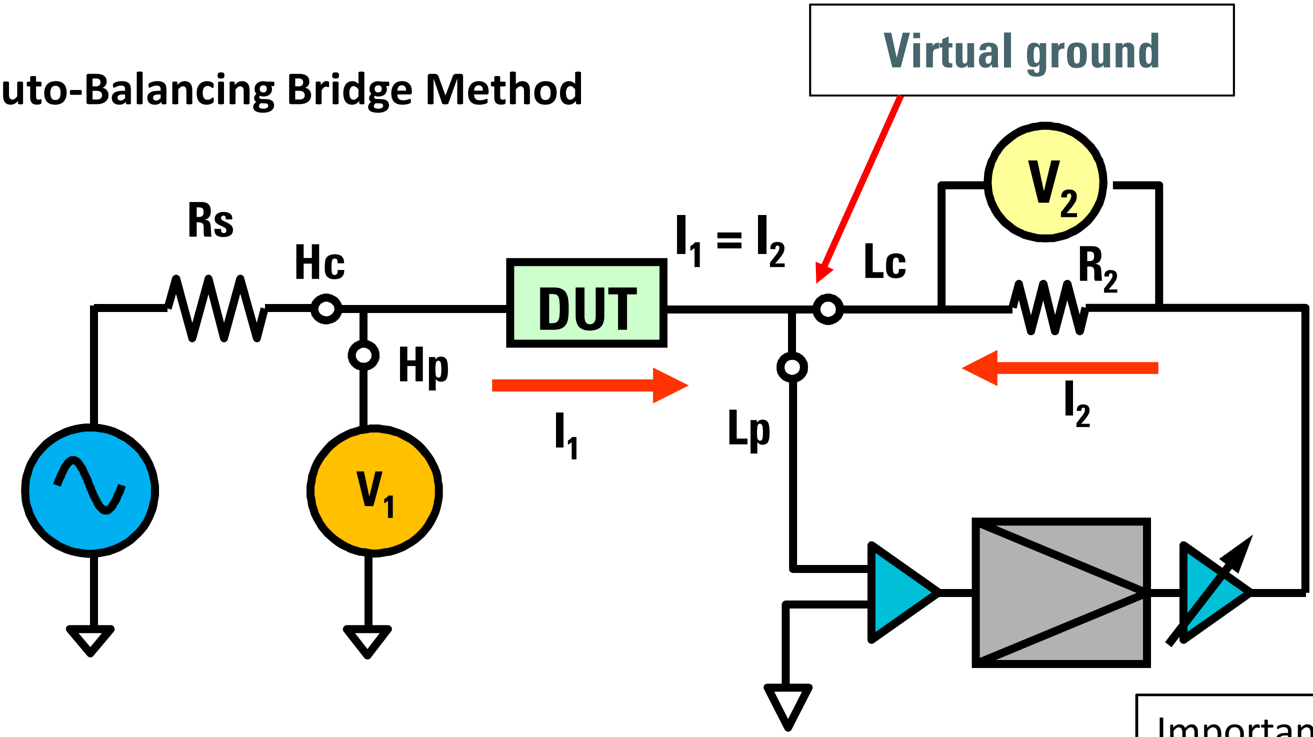


Junction capacitances vary with applied DC voltage, so you must measure them with thousands of volts of applied DC bias.

**Issue:** No off-the-shelf capacitance meter supports measurements with more than a few tens of volts of DC bias.

# How Does a Capacitance Meter Work?

**Auto-Balancing Bridge Method**

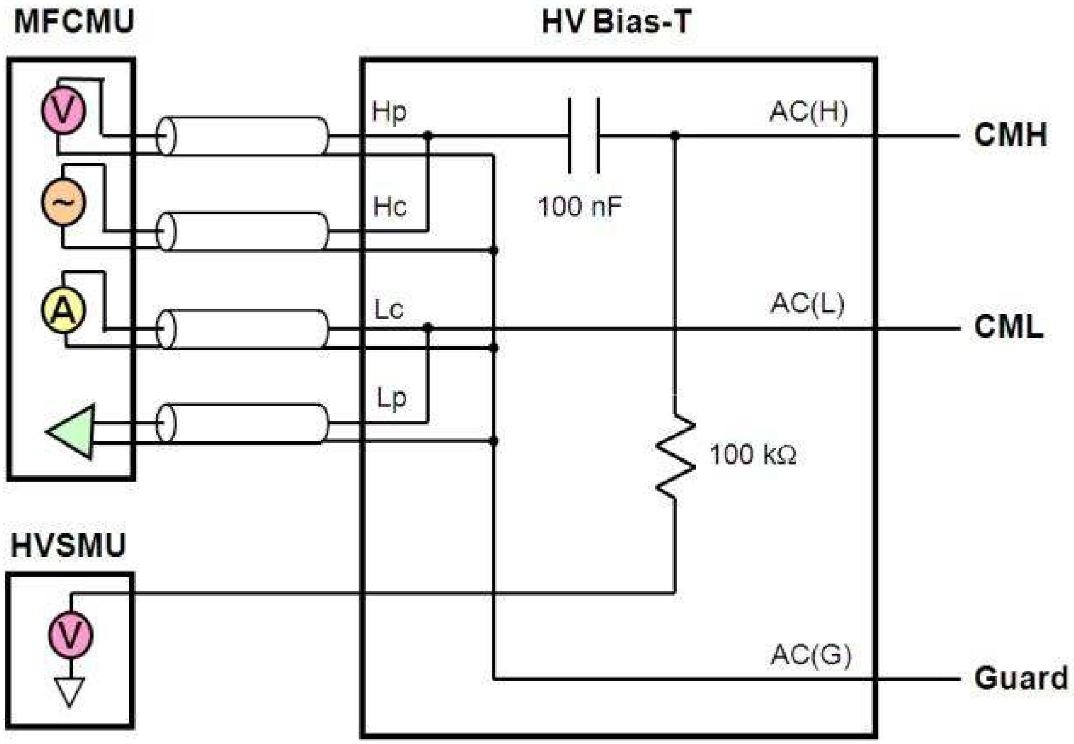


$$V_2 = I_2 \times R_2$$

$$Z = \frac{V_1}{I_2} = \frac{V_1 R_2}{V_2}$$

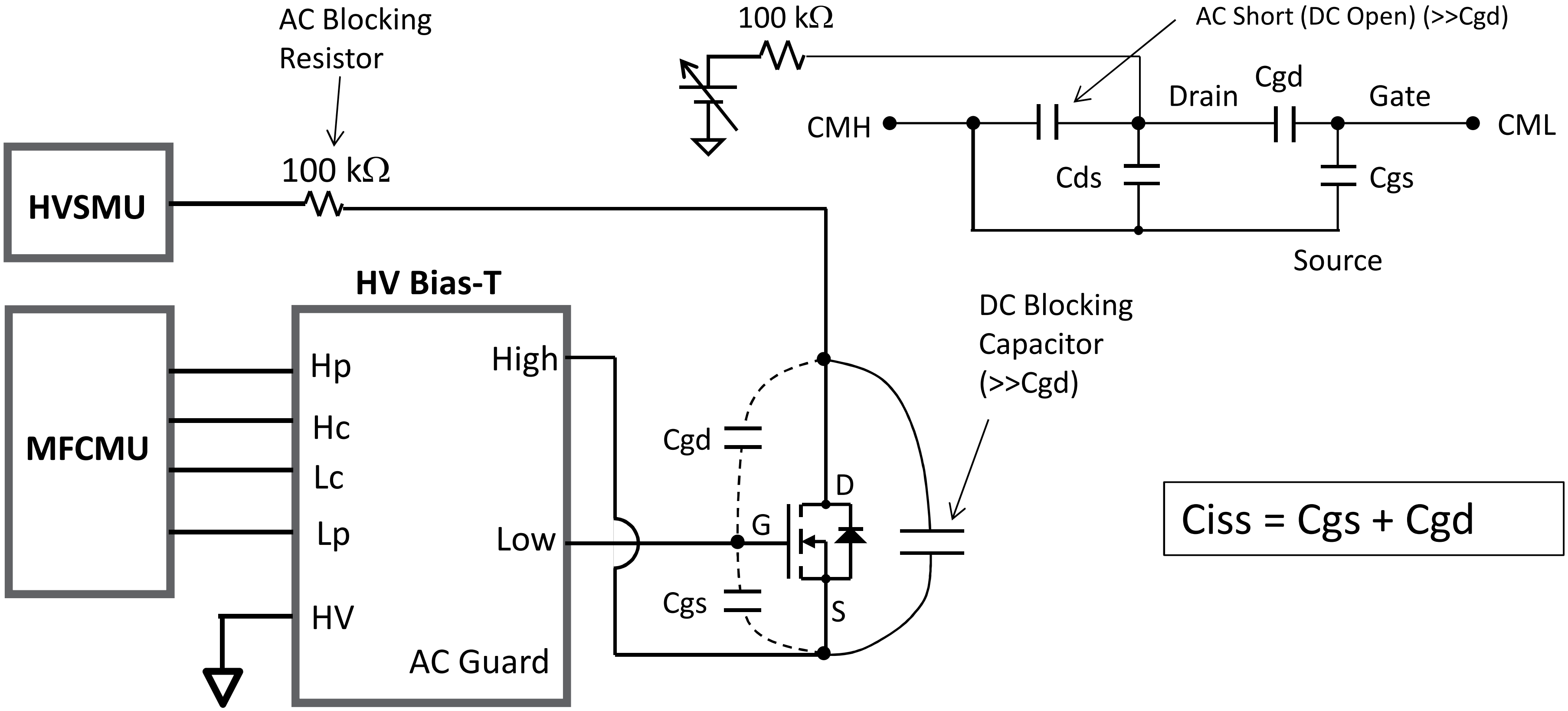
Important! The measurement is made at the Lp and Lc terminals.

# High-Voltage Bias-T Measures Capacitance at 3 kV



The DC bias can be at thousands of volts while the AC signal is in the tens of millivolts.

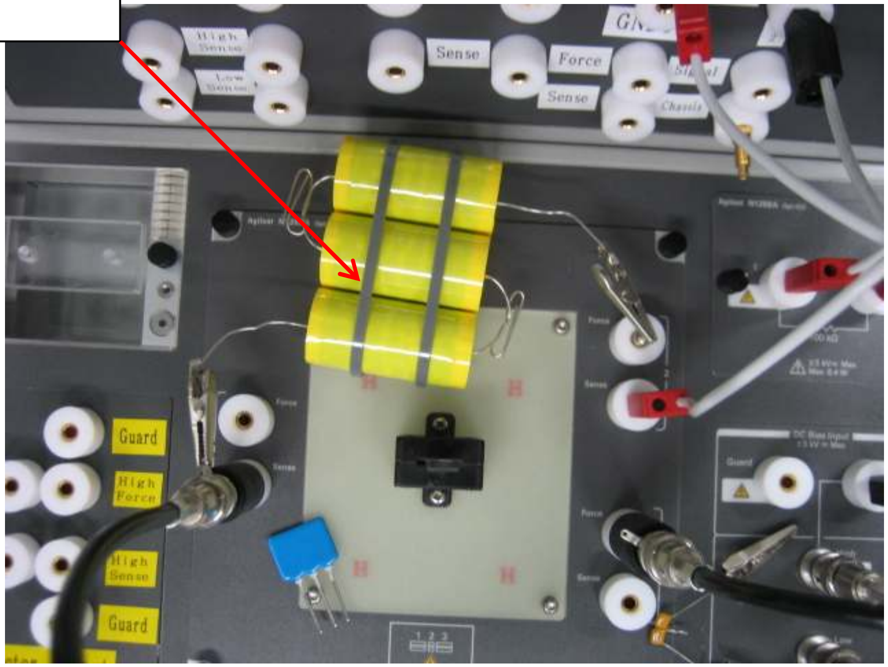
# Measurement Example – Ciss (Normally Off Device)



Ciss = Cgs + Cgd

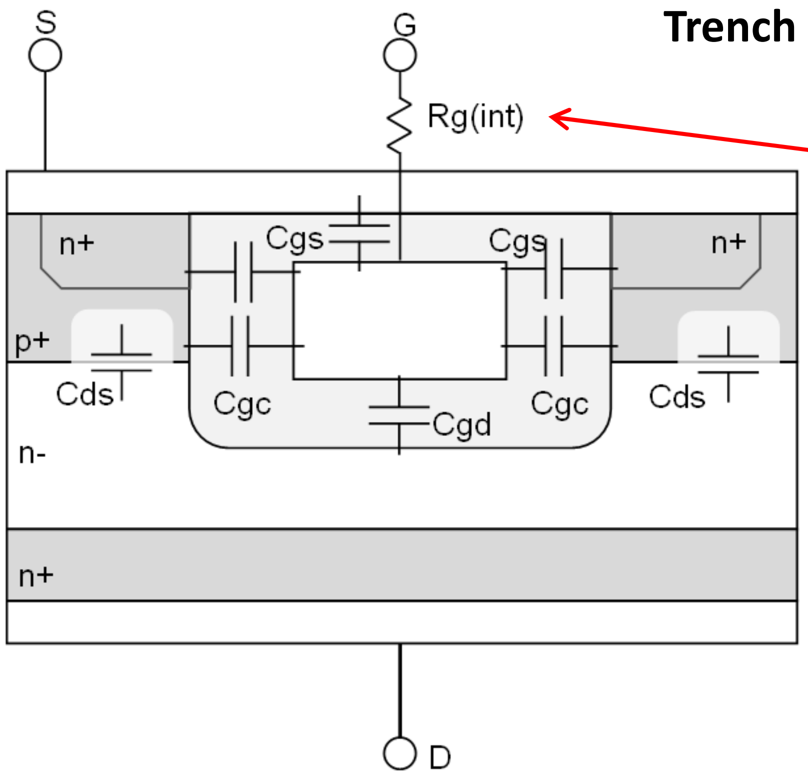
# Examples of Typical Blocking Capacitors

The capacitors necessary to provide DC signal blocking can be quite large physically.



# What is Gate Resistance?

**Trench MOSFET Example**



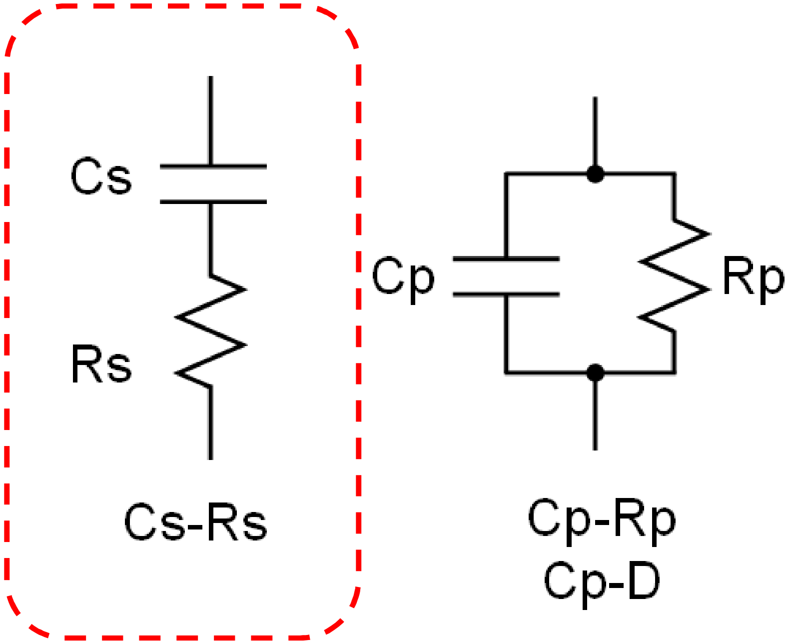
Gate resistance is the internal resistance of the transistor. In the example shown on the left, you can see that Rg is in series with three different internal capacitances:

1. Cgs (gate to source capacitance)
2. Cgd (gate to drain capacitance)
3. Cgc (gate to channel capacitance)

# How is Gate Resistance Measured?

Gate resistance is measured using an LCR meter, which is why it falls under the umbrella of capacitance measurement.

To determine Rg, we use the Cs-Rs model built-in to the LCR meter.

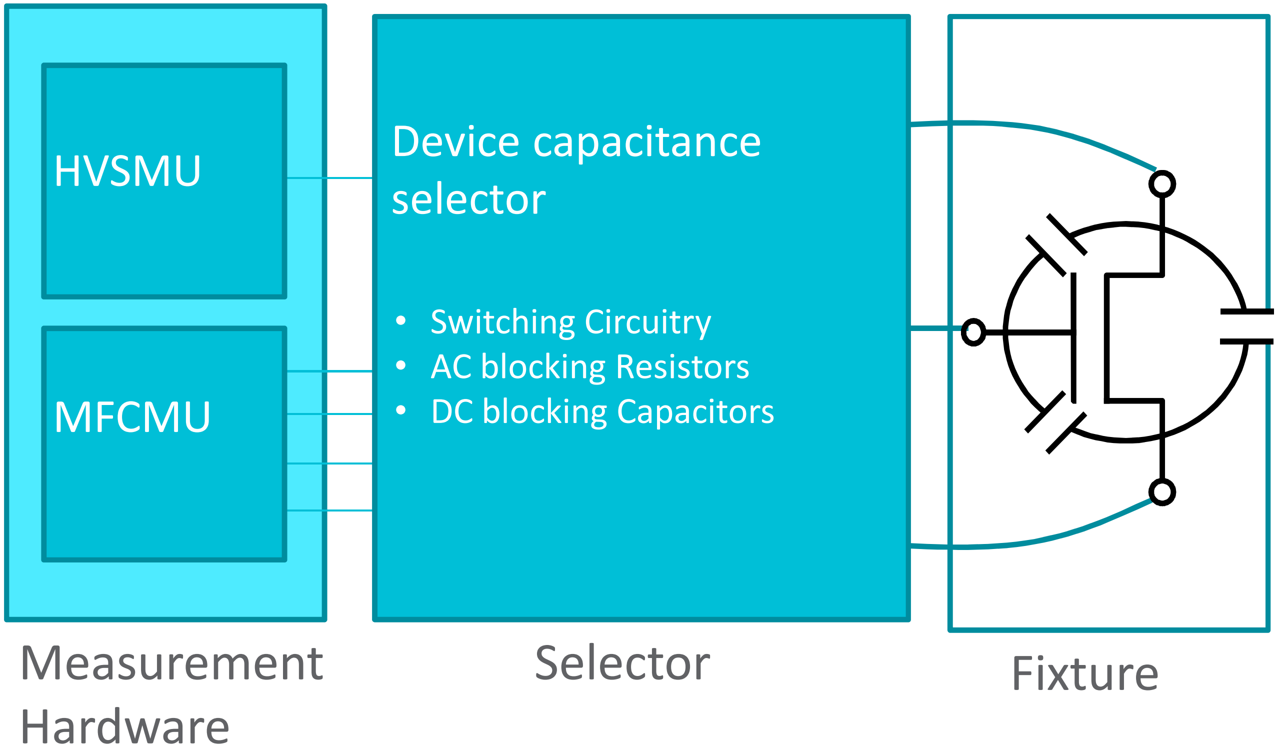


**LCR meter measurement modes**

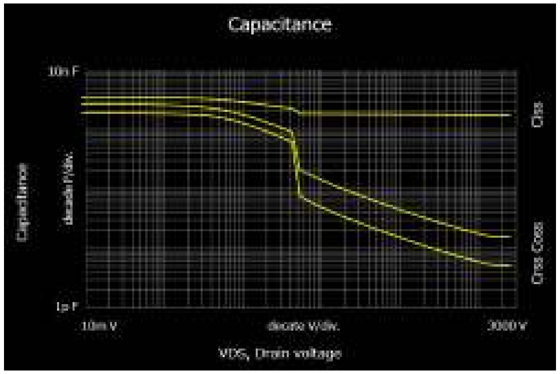
# Capacitance Measurement is Extremely Difficult!

- Each capacitance measurement requires some manual re-wiring of the test setup.
- The connections for each measurement can be quite complicated & require external components.
- Especially difficult to measure “normally on” devices.
- No easy way to automate Ciss, Coss and Crss measurement.
- A deep understanding of measurement theory is needed to get valid results.

# What is the Ideal Solution?



- Switching Circuitry
- AC blocking Resistors
- DC blocking Capacitors



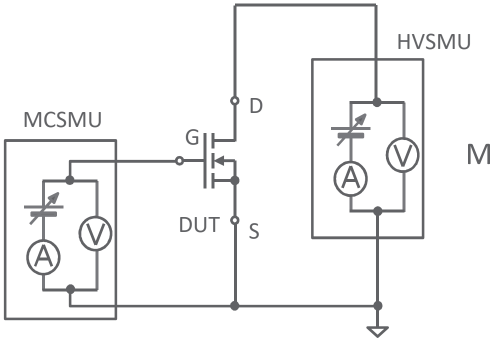
Power MOSFET capacitances can be measured up to 3 kV in a few minutes without the need to change any connections.

**Switching Matrix + Additional Components + Software**

# Agenda for Today

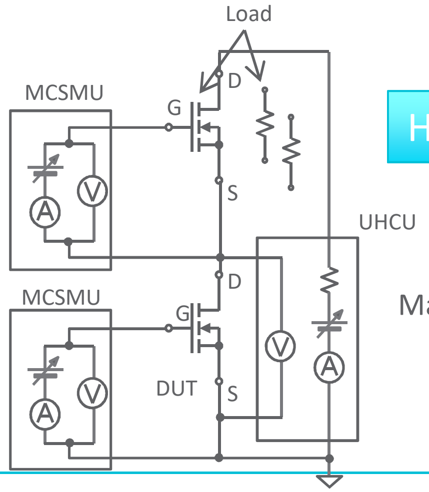
1. *Why Use Wide Band Gap Devices?*
2. *Calculating Power Loss in Power Semiconductor Devices*
3. *Measuring Power Device Capacitance*
4. *Measuring Power Gate Charge*
5. *Power Analysis for Energy Conversion Devices*

# The Two-Pass Gate Charge Measurement Method



High Voltage Part

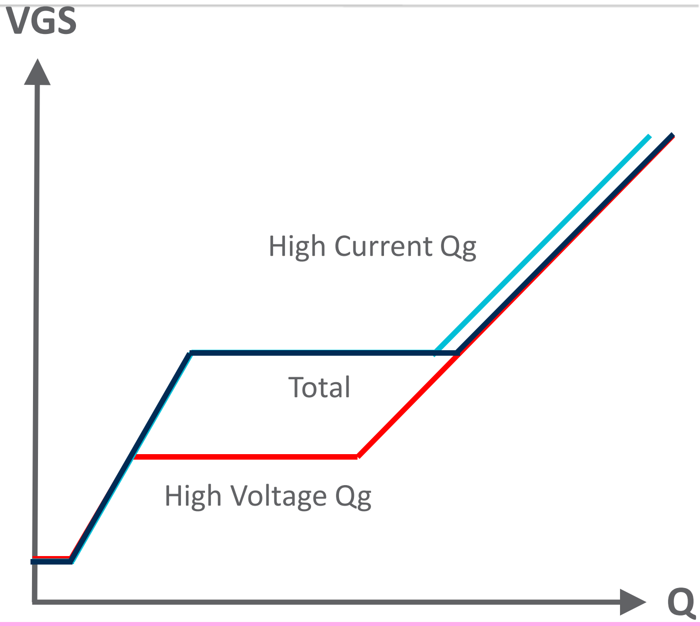
Max. 3 kV, 4 mA



High Current Part

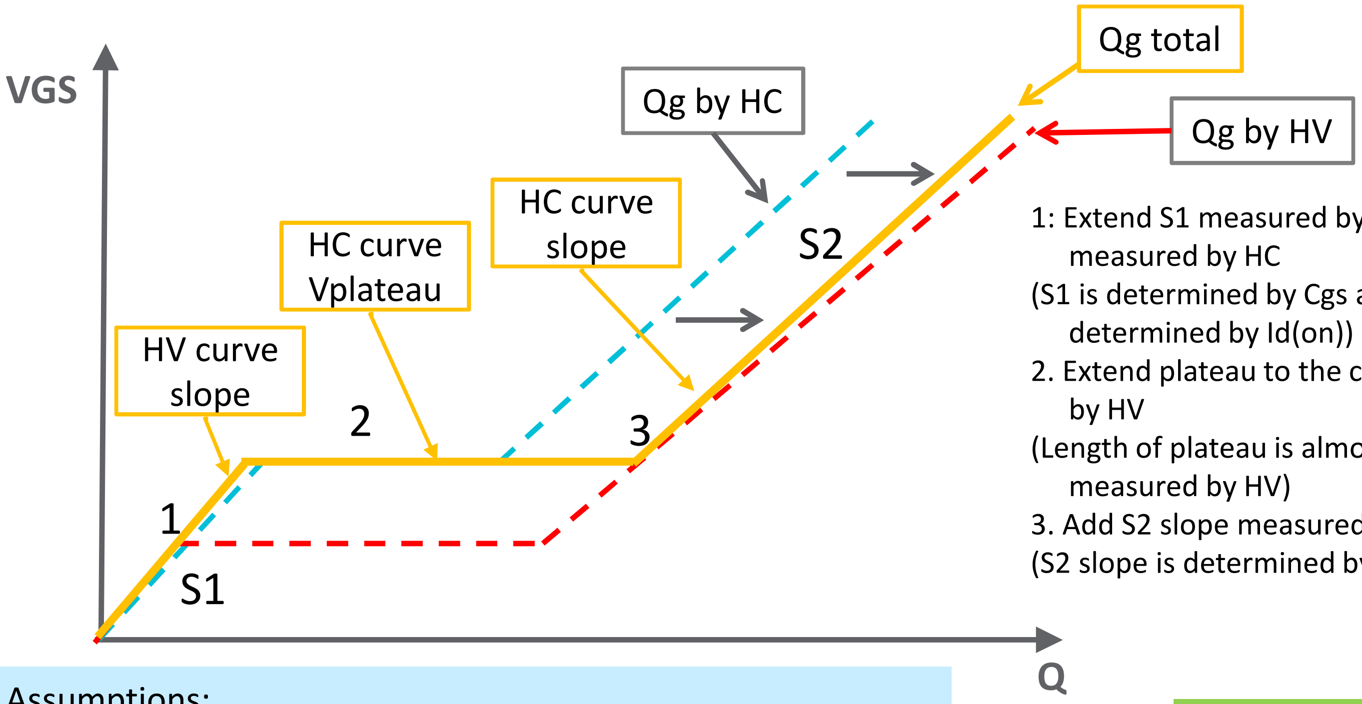
Max. 1500 A, 60 V

Combine
Max 3kV/1500A



- Measure Qg at high current/low voltage and high voltage/low current separately.
- The two curves are then merged to create the gate charge curve at the desired current and voltage.

# Details of Two-Pass (HV/HC) Method



1: Extend S1 measured by HV to the plateau voltage measured by HC

(S1 is determined by Cgs at Vd(off) and Vgs(pl) is determined by Id(on))

2. Extend plateau to the cross point with the S2 slope by HV

(Length of plateau is almost same as the plateau measured by HV)

3. Add S2 slope measured by HC

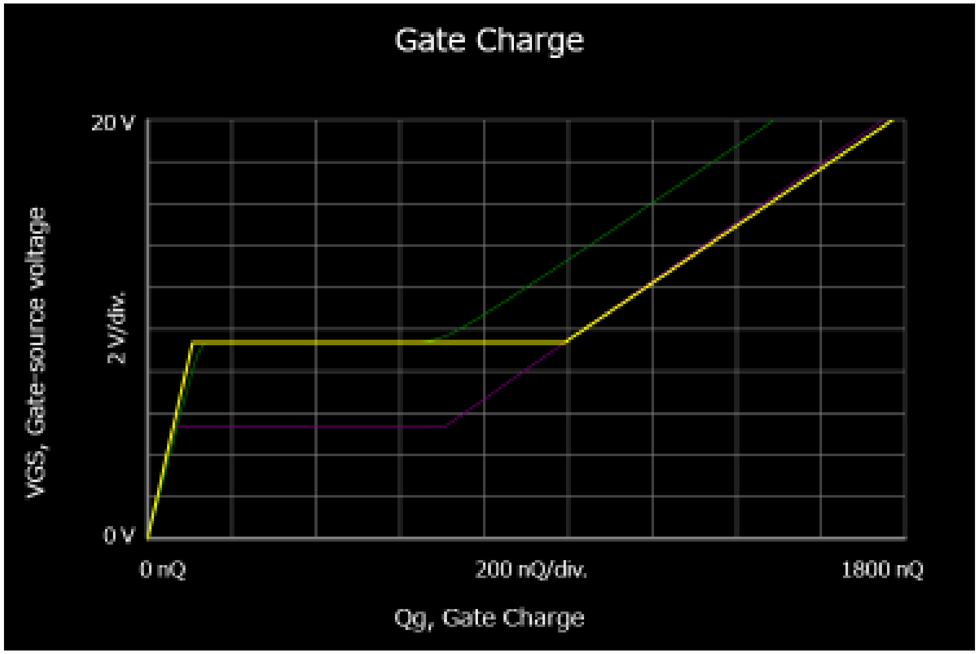
(S2 slope is determined by Ciss at Id(on))

Assumptions:

- Cgs (off) and Ciss (off) are almost the same at HC and HV
- Difference of Vds(on) between HC and HV are negligible

Reasonable for switching devices used in converter/inverter

# Two-Pass Gate Charge Measurement Example



- ❖ Supports all power devices up to 3 kV, breaking previous 60 V limit for commercially available $Q_g$ test equipment
- ❖ Easily evaluate $Q_g$ character-istics of high current and high voltage devices such as IGBT modules
- ❖ $Q_g$ characteristics along with other measured parameters can be used to automatically calculate power losses

# On-Wafer Gate Charge Measurement Issues

- Select a current load FET of appropriate size (not too much larger than the DUT).

- Twist the high force and low force cables together.

- Attach ferrite cores around the gate probe needle as close to the DUT as possible.

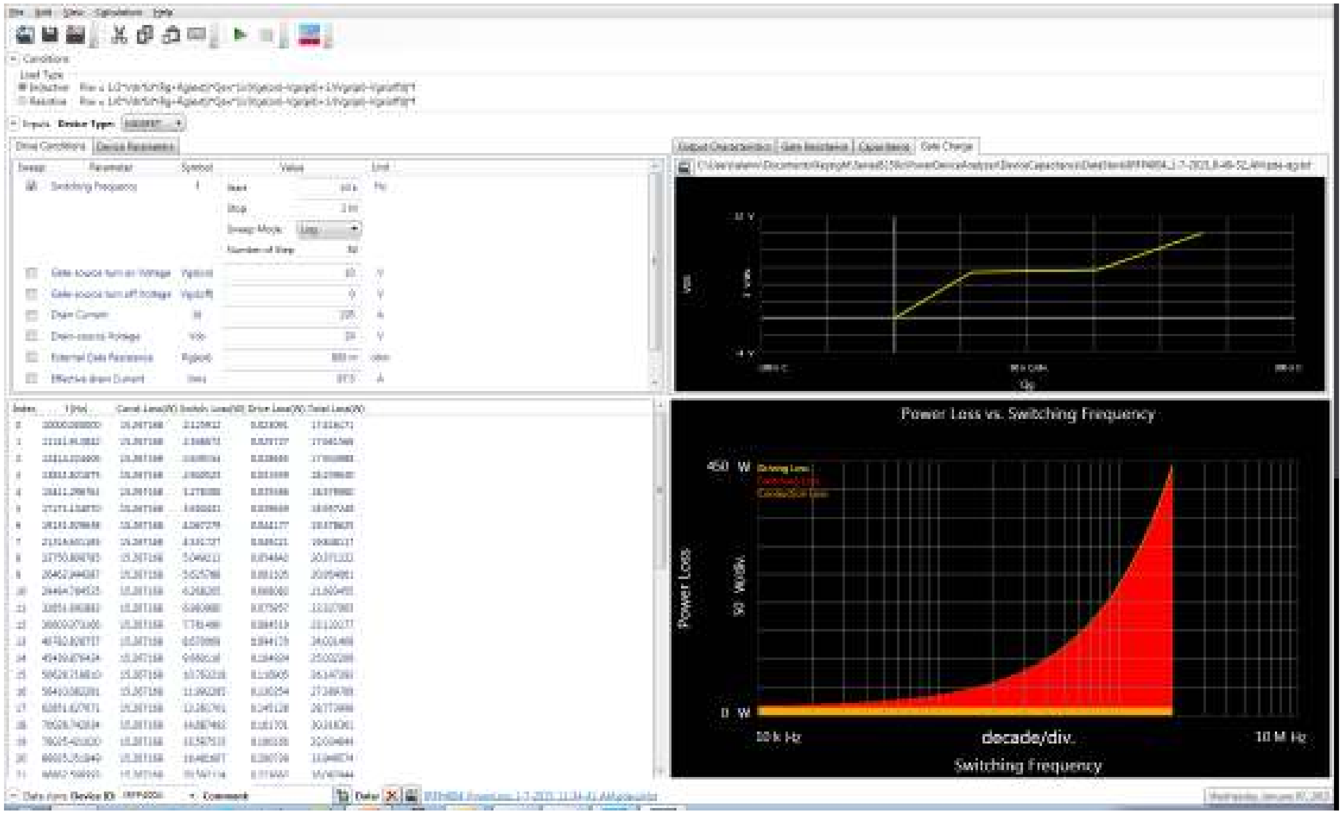
- Attach a capacitor between the gate and the source as close to the DUT as possible.
- Perform Qg adapter calibration with the capacitor in-place.

Preventing oscillation is of primary importance when making on-wafer gate charge measurements.

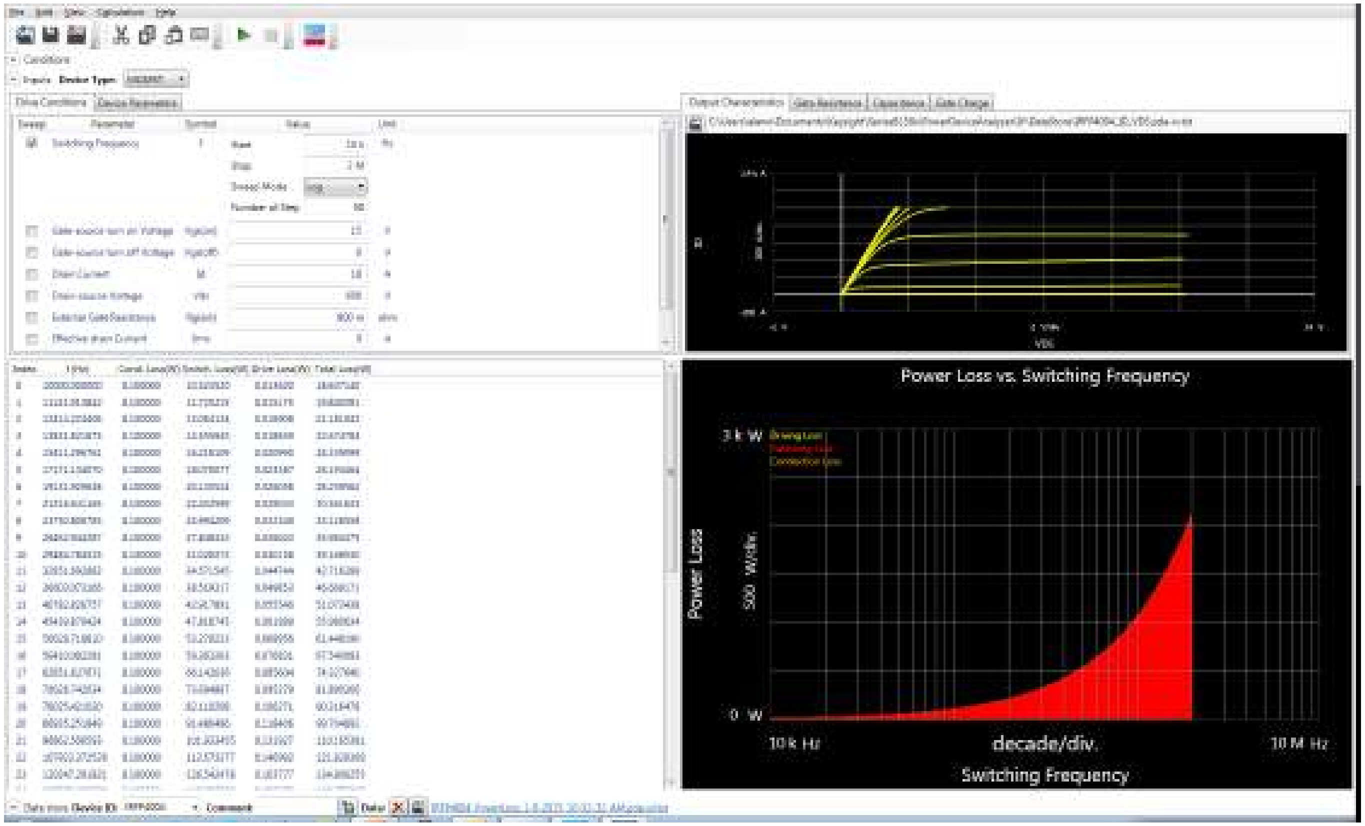
# Agenda for Today

1. *Why Use Wide Band Gap Devices?*
2. *Calculating Power Loss in Power Semiconductor Devices*
3. *Measuring Power Device Capacitance*
4. *Measuring Power Gate Charge*
5. *Power Analysis for Energy Conversion Devices*

# Sample Power Loss Calculation on Si MOSFET



# Sample Power Loss Calculation on SiC Device



Notice that there is virtually no conduction loss.

# Thank You!

**For questions, please contact:**

Joshua Sarris

Keysight Technologies

Joshua.sarris@keysight.com

(408) 236-6047