# Silicon Photonics Reliability and Qualification Testing

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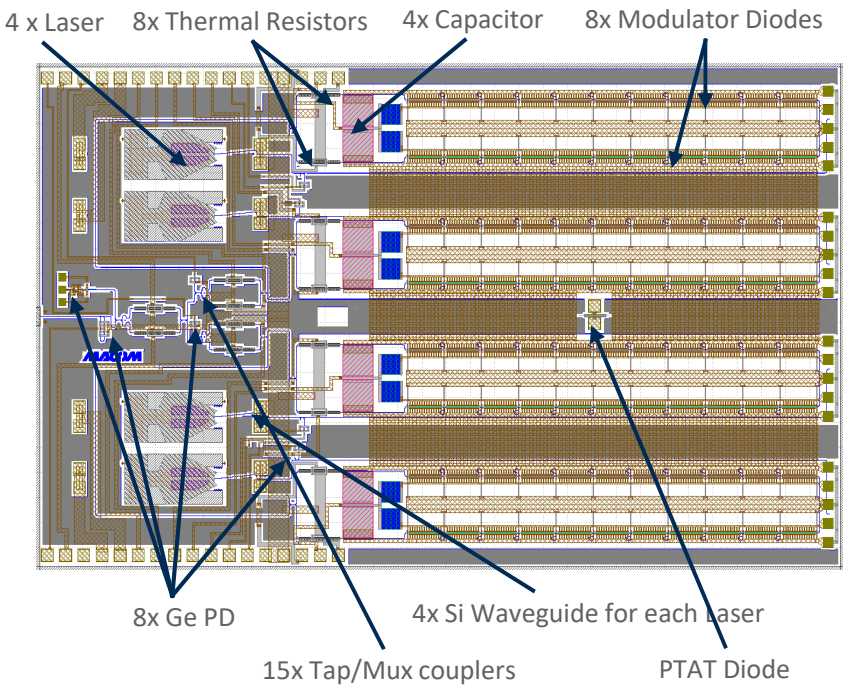
# Agenda

1. *Silicon Photonics Design and Process Overview - Challenges*
2. *Silicon Photonics Reliability and Qualification Test Matrix*
3. *FormFactor 1164 Reliability test system*
4. *Going Forward – FormFactor Testing*
5. *Wafer Probing Considerations – End User Requirements*
6. *Conclusion*

# 1. Silicon Photonics Design and Process Overview

- Silicon Photonics Transceiver Value Proposition:
  - Power reduction
  - Size reduction
  - Performance, higher data throughput
  - IC CMOS Tools
  - Optics Integration
  - Lower Optics Costs
- *Achieve a level of integration, manufacturability, Scalability (Cost/Power/Size) for optics, in line with CMOS Electrical ICs by leveraging existing CMOS Design, fabrication, manufacturing infrastructure.*
- *Make optics more mainstream.*



# 1. Silicon Photonics Design and Process Overview

| Silicon Photonics Design Commonalties | Silicon Photonics Design Differences |
|---|---|
| **Optical** | **Optical** |
| Laser sources | Laser coupling: direct, lens and isolator elements, hybrid growth on SiPh Die. |
| Photodiodes (PD) | Coupling of waveguide to PD. Direct, Adiabatic, Si, Si Ni. |
| Waveguides: Si, Poly Si, Silicon Nitride, Couplers, MUX/DEMUX | Coupling schemes between WG and couplers, mux/demux and PD. |
| Design lay-out:<br>Use of standardized CAD tools.<br>Use library based cell design approach. | Unique to supplier design and foundry wafer manufacturer |

- Unique to designer: lay-out, size, length, dopant profiles and foundry partner.
- No foundry industry defined component and process PDK available.
- Testing, Reliability and qualification testing falls to the end user and supplier.
- **HOWEVER: Foundry device element and process PDK in the works.**

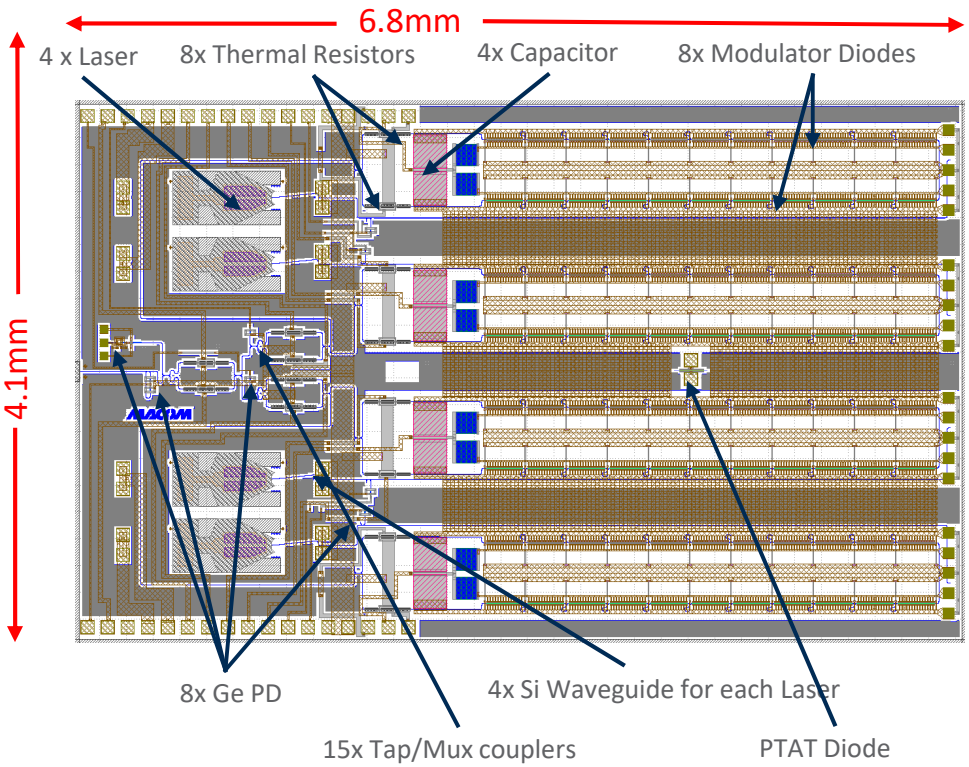
# 1. Silicon Photonics Design and Process Overview

| Silicon Photonics Design Commonalties | Silicon Photonics Design Differences |
|---|---|
| **Electrical** | **Electrical** |
| Modulator structure: ie: diode, SISCAP. | **Unique to designer: lay-out, size, length, dopant profiles and foundry partner.**<br><br>**No foundry industry defined component and process PDK available.**<br><br>**Testing, Reliability and qualification testing falls to the end user and supplier.** |
| Capacitors | |
| Resistors: thermal modulator and MUX/DEMUX tuning | |
| Photodiodes | |
| Temperature sensors | |
| Wirebond and test pads | |
| Design lay-out:<br>Use of standardized CAD tools.<br>Use of standard electrical CMOS IC design flow.<br>Use library based cell design approach. | |

# 2. Silicon Photonics Reliability and Qualification Test Matrix

**Rel/Qual program consists of four parts:**

1. *Discrete device (Mod. Diode, Cap, Ge PD, Thermal resistor) Lifetime predictions (Reliability) (FormFactor 1164 Tester)*
2. *Bare die (no laser) full electrical stressing of the die. (Opportunity for Form Factor)*
3. *Assembled (with laser) full optical/electrical stressing of the die. (Opportunity for Form Factor)*
4. *Mechanicals: Wirebond pad integrity, laser attach integrity.*



# 2.1 SiPh Discrete Device and Lifetime Predictions

- *Test objective: To use accelerated reverse bias voltage and temperatures to extract a lifetime reliability model for the discreet components: Mod. Diode, Cap, Ge PD, Thermal resistor, PTAT*
- *Sample sizes: at minimum 192 samples of each component at 4 voltages and two temperatures.*
- *Record times to failure, generate CDF plots and solve for Ea and N factor in Power Law model.*
- *FormFactor 1164 system excels at this type of testing.*
- *Testing is used to determine intrinsic/extrinsic failure mode voltage levels.*

Sample Test Matrix

| Voltage Stress (V) | Stress Temperatures (C) | |
|---|---|---|
| | 95 | 125 |
| V1 | | 192 |
| V2 | | 192 |
| V3 | 192 | 192 |
| V4 | | 192 |

# 2.2 SiPh Bare Die (No Laser or Optics)

- Test objective: Using JEDEC electrical level testing conditions, stress the full product die to verify if there are any interactive failure modes in the fully assembled functional modulator on chip.
- (Opportunity for FormFactor)

| Cell # | Tests | Reference | Test Conditions | Test Intervals | Sample Size |
|---|---|---|---|---|---|
| 1 | High temperature Operating Life 1,2,3 | JESD92<br>JEP001A | Typical, HTLV and LTHV Field Conditions:<br>Ambient Temperature = 85C, 125C<br>Modulator Diode, Integrated Ge PD, Term Cap, PTAT and Thermal Resistors are biased. | T0, 168, 500, 1000, 1500, 2000, 3000, 4000, 5000hrs. | Pick total number of dies that will give a minimum number of components:<br><br>Each group will test 240 Mod. Diodes, 210 Ge PDs, 240 thermal resistors and 120 Term Caps |
| 4 | High Temperature Storage | JEP001A | Ambient Temperature = 150C | T0, 168, 500, 1000, 1500, 2000hrs. | |
| 5 | Damp Heat (unbiased) | GR-468 | Ambient Temperature = 85C<br>Relative Humidity = 85% | T0, 168, 500, 1000, 1500, 2000, 3000, 4000, 5000hrs. | |
| 6 | Damp Heat (biased) | GR-468 | Typical Field Conditions:<br>Ambient Temperature = 85C, 125C<br>Relative Humidity = 85%<br>Modulator Diode, Integrated Ge PD, Term Cap, PTAT and Thermal Resistors are biased. | | |
| 7 | Temperature Cycling | JEP001A | -55C to 125C, 15 min dwells, 5C/min ramp rates | T0, T100, T250, T500, T750, T1000 cycles. | |
| 8 | ESD Human Body Model Characterization | JEDEC JS-001-2017 | Expected minimum ESD level to be 0A to 1B. | Start at 100V, increment in 50V steps. | 6 devices at each voltage level. |

# 2.2 SiPh Bare Die (No Laser or Optics)

- Pass/fail criteria - Typical parameters measured:

| Parameter | Pass/Fail Criteria | Measured at: |
|---|---|---|
| Modulator Diode Reverse Bias Leakage Current | < xx nA | Low, operating and high Voltage |
| Ge PD detector dark current | < xx nA | |
| Term Cap Leakage Current | < xx nA | |
| Thermal Resistor | +/-5% ~ +/- XX Ohm | Resistance measured. |
| PTAT | +/- xx mV/C | Room temperature only |

- Pre and post measurements @25C only.
- All pass/fail criteria are all DC measurements, no RF measurements needed for reliability determination of the SiPh chip. RF measurements solely needed to validate design functionality.
- All pass/fail criteria are unique to the particular chip design, supplier and compensating / functional limits of the electrical driver ICs that will be paired with the SiPh chip.

# 2.3 SiPh Assembled Die (With Laser and/or Optics)

- Test objective: Using Telcordia optical level testing conditions, stress the full product die with lasers to verify if there are any interactive failure modules due to optics when assembled as a fully functional modulator. In addition to electrical parameters, also used to demonstrate long-term modulator stability of the Si waveguides, nanotapers, couplers, MUX and modulator phase.
- (Opportunity for FormFactor)

| Cell # | Tests | Reference | Test Conditions | Test Intervals | Sample Size |
|---|---|---|---|---|---|
| 1 | High temperature Operating Life | GR-468 | Typical Temperature and Bias:<br>Ambient Temperature = 85C<br>Laser bias = at BOL current<br>Modulator Diode, Integrated Ge PD, Term Cap, PTAT and Thermal Resistors are biased. | T0, 168, 500, 1000, 1500, 2000, 3000, 4000, 5000hrs. | Pick total number of dies that will give a minimum number of components:<br><br>Each group will test 240 Mod. Diodes, 210 Ge PDs, 240 thermal resistors and 120 Term Caps |
| 2 | Temperature Cycling | GR-468 | -40C to 85C, 15 min dwells, 5C/min ramp rates | T0, T100, T250, T500, T750, T1000 cycles. | |
| 3 | Damp Heat (unbiased) | GR-468 | Ambient Temperature = 85C<br>Relative Humidity = 85% | T0, 168, 500, 1000, 1500, 2000, 3000, 4000, 5000hrs. | |
| 4 | Damp Heat (biased) | GR-468 | Typ. Temp. Accelerated Bias:<br>Ambient Temperature = 85C<br>Laser bias = threshold +10% mA<br>Modulator Diode, Integrated Ge PD, Term Cap, PTAT and Thermal Resistors are biased. | | |
| 5 | Low Temperature Storage | GR-468 | Ambient temperature = -40C | T0, 168, 500hrs | 12 L-PIC Dies |

# 2.3 SiPh Assembled Die (With Laser and/or Optics)

- Pass/fail criteria - Typical parameters measured:

| Parameter | Pass/Fail Criteria | Measured at: |
|---|---|---|
| LI curve using Input PDs | < 0.5dB change | Laser current: 0 to Ibias max ma, increment 0.5mA.<br>Plot at 100ma Laser Bias.<br>(short modulator diode during measurement) |
| LI curve using Post Modulator PD | < 0.5dB change | |
| Modulator Loss:<br>• = Input PD – Modulator Output PD | < 0.5dB change | Plot at 100ma Laser Bias (short modulator diode during measurement) |
| Generate MZI Curves for each modulator to evaluate modulator phase stability | <+/- x.xx radians | Generate curves with Laser Bias at fixed Ibias mA.<br>Sweep one thermal resistor from 0 to max power to generate curve.<br>Read modulator output PD current response to generate curve.<br>Fit sine wave response and extract phase information. |
| Measure SMSR and Ith of each laser | <+/- ???? | Measure at same laser currents as in production during the LIV curve generation above. |

- Pre and post measurements @25C only.
- All pass/fail criteria are all DC measurements and passive optical, no RF measurements needed for reliability determination of the SiPh chip. RF measurements solely needed to validate design functionality.
- All pass/fail criteria are unique to the particular chip design, supplier and compensating / functional limits of the electrical driver ICs that will be paired with the SiPh chip.

# 2.4 SiPh Mechanicals – Wirebond Pad and Laser Attach Integrity

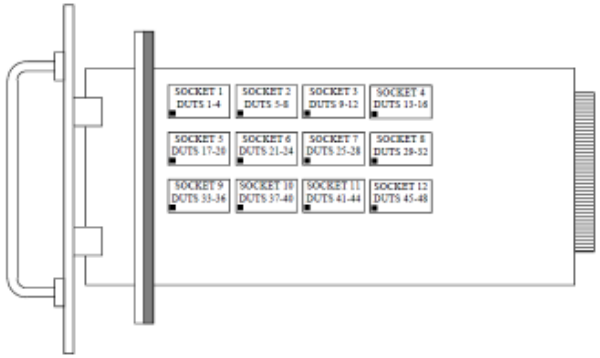
- *Wirebond pad integrity and laser attach integrity.*

| Tests | Reference | Test Conditions | Sample Size | Comments |
|---|---|---|---|---|
| Initial Wire Bond Pulls | Mil-STD-883J-Method 2011.7 | 3g for 0.7 mil, 6g for 1 mil wire. | 12 SiPh die. | Wirebond pad to pad. |
| Initial Wirebond Ball shears | JESD22-B116A | Pass criteria is dependent on wirebond ball diameter. TBD from standard. | | Shear ball after wirebond pull test. |
| Initial Laser attach shears | Mil-Std 883 Method 2019.6 | Laser attach area = TBD | | |
| Temperature cycling | GR-468 | -40C to 85C, 15 min dwells, 5C/min ramp rates, 100, 250, 500 cycles. | 6, 6, 6 = 18 die. | Remove samples from chamber and wirebond pull and then shear WB ball at each interval. Do laser shears as well. |
| Unbiased Damp Heat | GR-468 | Ambient Temperature = 85C<br>Relative Humidity = 85%<br>T500, 1000hrs, 2000hrs | 6, 6, 6 = 18 die. | |

- 48 total samples needed.
- Generate CDF plots.
- Pass criteria = Shear and pull distributions to pass minimum criteria with < 0.01% population failure at 90% confidence.

# 3. FormFactor 1164 Reliability Test System

- *Test Equipment Requirements for SiPh Discrete Components and Lifetime Predictions:*
- *The FormFactor 1164 Reliability Tester excels at this type of testing.*


## 230°C High-Current / High-Accuracy TDDB DUT Board

| | Part Number | Description |
|---|---|---|
| Final Assembly: | 166-550 | ASSY,DB,HI/HATDDB,230,600,24,12S |

| | |
|---|---|
| PC Board Material: | Polyimide |
| Package Size: | 600-mil 24-pin DIP |
| Number of DUTs: | 48 (12 x 4) |
| Max Temperature: | 230°C |

***Note:***

This DUT board is used with either High Current or High Accuracy TDDB application modules in a High Current 4Pak.

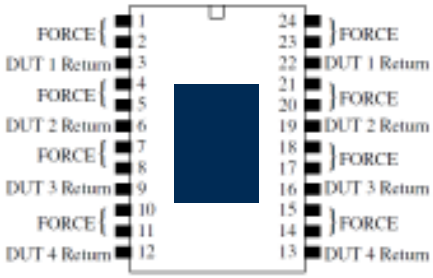
**Package Layout**

Signals are assigned to socket pins according to the following table.

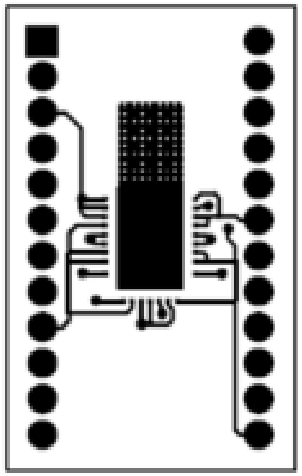
| Pin No. | Signal | Description |
|---|---|---|
| 3, 22 | DUT1 RTN | Ammeter 1 input (virtual ground) |
| 6, 19 | DUT2 RTN | Ammeter 2 input (virtual ground) |
| 9, 16 | DUT3 RTN | Ammeter 3 input (virtual ground) |
| 12, 13 | DUT4 RTN | Ammeter 4 input (virtual ground) |
| 1, 2, 4, 5, 7, 8, 10, 11, 14, 15, 17, 18, 20, 21, 23, 24 | FORCE | Shared Force voltage |

# 3. FormFactor 1164 Reliability Test System

- *Test Equipment Requirements:*
- *Custom designed PCB to fit 1164 system Socket.*




FF 1164 System Socket



Macom CWDM4 Test PCB

- Au Bond Pads
- Wirebond pads
- SiPh CWDM4 Die attached to PCB
- Die components wirebonded to DUT/Force pads/pins for stress testing.

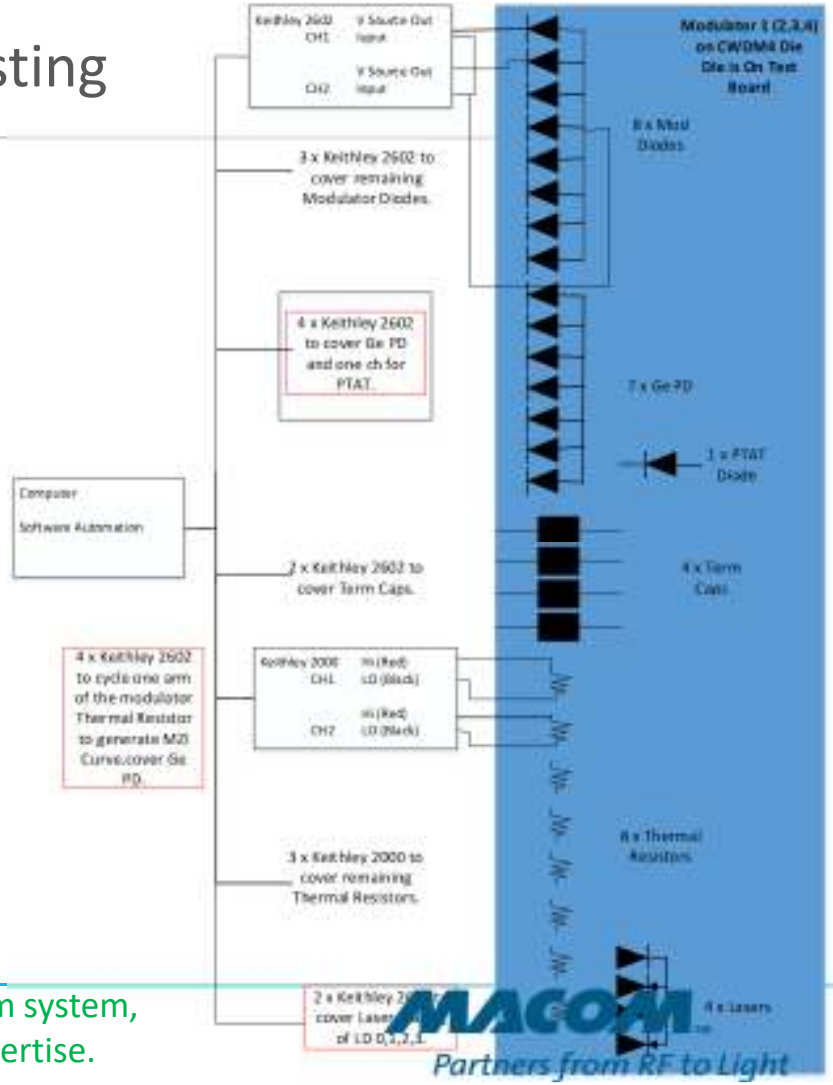
# 3. FormFactor 1164 Reliability Test System

- *Test Equipment Requirements for SiPh Discrete Components and Lifetime Predictions:*
- *The FormFactor 1164 Reliability Tester excels at this type of testing.*

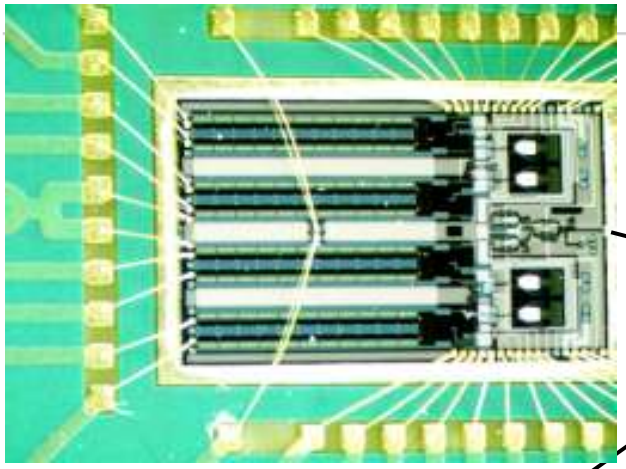
| Advantages | Disadvantages |
|---|---|
| Able to stress large # of samples, able to quickly get statistically significant sample sizes tested | Only one: Constant Current stress system was out of budget.<br><br>Form Factor can address this by reducing system accuracy and stability, especially for SiPh based testing. |
| Expandable | |
| Fully Automated with software | |
| Supplier support for Cal and repair is excellent | |
| Accuracy and stability is excellent for this testing | Not needed for SiPh testing, but consider pre/post measurement cold temperature (0 °C)capability. |
| Allows pre and post testing of devices at temperature | |
| Cost of test vehicle set-up is reasonable | |
| Voltage Stress system affordability is within budget | |

# 4. Going Forward FormFactor - SiPh Testing

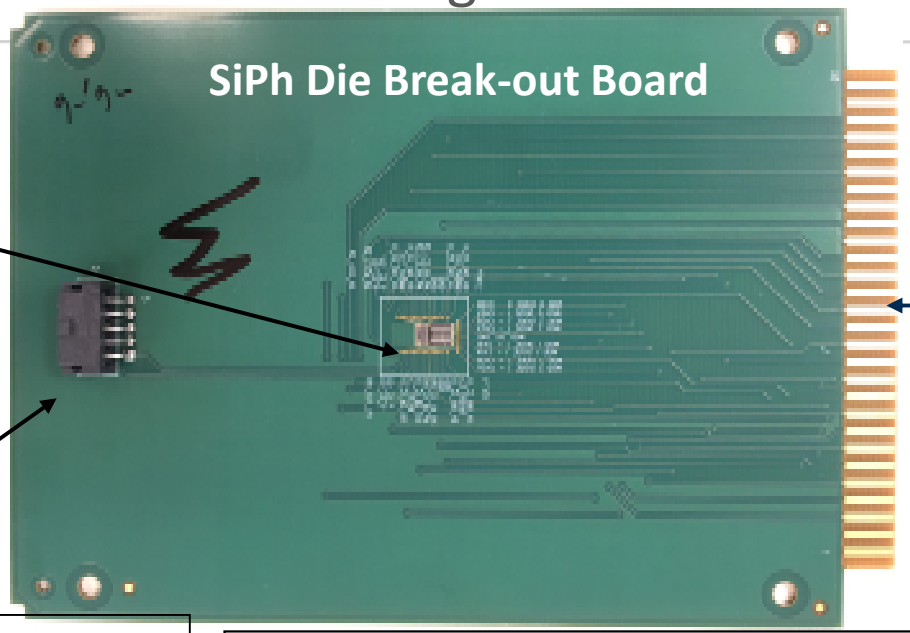
- **Bare and Assembled Die Pre/Post Stress Testing:**
- Made of 18 dual channel Keithley 26002 SMUs and one Keithley Multi-channel resistor measurement card.
- Computer driven with in house custom software automation.
- **FormFactor Opportunity:**
- Use existing 1164 SMU.
- SMUs must have high impedance mode to support common cathode laser configurations and common ground electrical elements.
- Use existing 1164 constant current drives with mA accuracy, 0 to 300mA range.
- SMU outputs to connector so user can add cabling to their test cage and backplane.
- Use existing 1164 software with modification.
- System is expandable.
- We prefer it since it eliminates our custom system, easier for upkeep and not our area of expertise.



# 4. Going Forward FormFactor - SiPh Testing



SiPh CWDM4 Die




- **For IN-SITU BIAS Testing.**
- All voltage biases are provided through the edge connector and cage backplane.
- Laser biases are provided through the added connector.

- **For Pre/Post Measurements.**
- SiPh Die Bonded on Au pad with Cu vias through PCB board for thermal conduction.
- Corresponding die pads wirebonded to wirebond pads on board.
- Laser and die component biases provided through the edge connector and cage backplane.

# 4. Going Forward FormFactor - SiPh Testing

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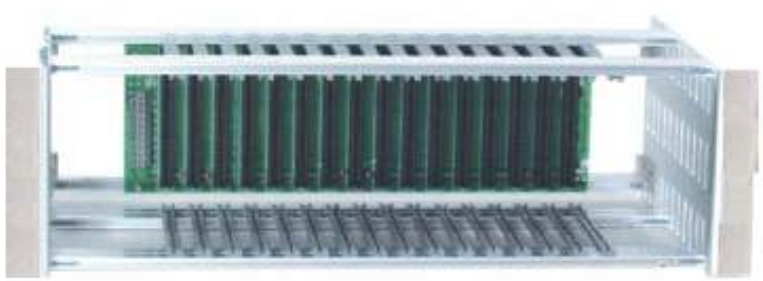


- Typical commercially available burn-in cages with backplanes.
- Come in 8 or 16 slot variants.

- Break-out board will serve two functions:
  - In-Situ Testing Bias: 16 break-out boards will slide into a burn-in rack, pictured on the left. All structures for all dies in the group will be biased by an external voltage/current source.
  - Pre/Post interval testing: Board is removed from the cage and each die is measured for parameters described in pass/fail criteria slide on the bare/assembled die tester.

# 5. Wafer Probing Considerations – End User Requirements

- SiPh Production wafers will have full reticles of end user SiPh dies and a KERF area.
- KERF area will serve 2 purposes:

1. Ongoing performance tracking (WAT – Wafer Acceptance Testing)
   - *Assess and track performance of every device used in product die*
   - *Process monitoring*
   - *Wafer acceptance*
   - *Should have same footprint on every wafer / tape-out*
   - *Can add variants as needed to reflect changes to product die.*
2. Engineering development
   - *New devices under development*

# 5. Wafer Probing Considerations – End User Requirements

- WAT AREA:
- Every device/cell used in product die must appear in the WAT area.

| Electrical WAT | Optical WAT | Lithographic/process |
|---|---|---|
| • All metals, vias, contacts<br>• Resistors and capacitors<br>• Thermal Devices | • Modulator<br>• Passives – tap, couplers, Y-splitter<br>• Ge detector<br>• Waveguide, bends, tapers<br>• Edge coupling | • All layers – for CDSEM – Inline Critical dimension tool or measured post FAB using TEM/FIB/SEM.<br>• SIMS – Dies for secondary ion mass spectrometry to verify dopant profiles for tool optimization. |

# 5. Wafer Probing Considerations – End User Requirements

- Electrical WAT AREA:
- List of devices vs. quantities measured:

| Device | Quantity | Test Configuration |
|---|---|---|
| Metal x | Sheet rho | VDP (van de Pauw structure) |
| Via x | resistance | VDP |
| Contact | resistance | VDP |
| Doped Si (n,n+,p,etc.) | Sheet rho | VDP |
| MIMCap | C(V) | indiv. device |
| Thermal Device | I(V) vs. temp | indiv. device |
| GePD | S11, C(V), dark current | indiv. device |
| Modulator | S11, C(V), leakage current | indiv. device |
| Thermal tuner | resistance | indiv. device |

# 5. Wafer Probing Considerations – End User Requirements

- Optical WAT AREA:
- List of devices vs. quantities measured:

| Device | Quantity | Test Configuration |
|---|---|---|
| Modulator | Loss/cm | 3 lengths of mod. |
| Waveguide | Loss/cm | 3 lengths of waveguide of each type |
| MMI | Loss, SR | Indiv. device |
| Y-splitter | Loss, SR | Indiv. device |
| Tap | Loss, Tap ratio | Indiv. device |
| Waveguide taper | Loss | Several in series |
| Waveguide bend | Loss | Several in series |
| Thermal tuner | Loss | Several in series |
| Interleaver | Transmission | Indiv. device |
| Echelle | Transmission | Indiv. device |

# 5. Wafer Probing Considerations – End User Requirements

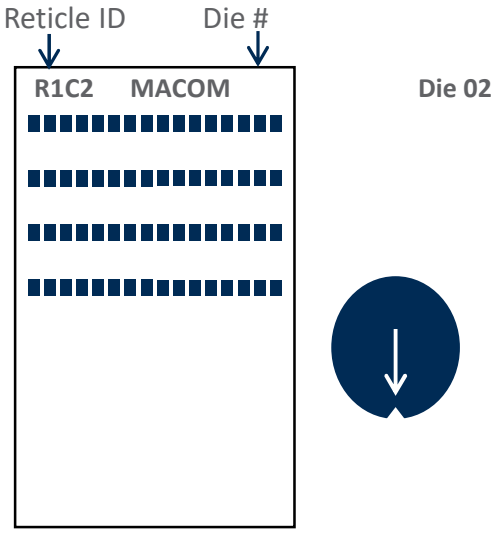
- Electro-Optical WAT AREA:
- List of devices vs. quantities measured:

| Device | Quantity | Test Configuration |
|---|---|---|
| Modulator | S21 BW<br>Loss/cm vs. V<br>Phase/cm vs. V | MZI |
| GePD | S21 BW,<br>Responsivity | Indiv. device |
| Thermal tuner | Phase vs. V or P | MZI |

# 5. Wafer Probing Considerations – End User Requirements

- Optical die waveguide layout:
  - Use edge coupling techniques to characterize waveguide types using transmission loss measurements.
  - If a grating coupler is available, wafer level testing can be performed using a defined pad cage. Dies with gratings can also be singulated and measured using die test techniques.

- Electrical die layout for DC measurements:
  - Each device has a unique numerical ID.
  - Pads are arranged in rows, always with horizontal orientation to the wafer notch.
  - Always use standard padset, e.g. 16 x 100µm pitch.
  - Align padsets vertically on each die to ease probing.
  - Pads should be tall to allow overdrive.



# 5. Wafer Probing Considerations – End User Requirements

| What parts of the REL/QUAL plan can be executed at wafer level? | |
|---|---|
| **Rel/Qual program requirement:** | **Wafer level testing – comments:** |
| **Discrete device** (Mod. Diode, Cap, Ge PD, Thermal resistor) Lifetime predictions (Reliability) | • Yes, wafers can be heated to temperature on the wafer chuck and can be probed electrically.<br>• Drawback, ties up a wafer prober for extensive amounts of time. |
| **Bare die** (no laser) full electrical stressing of the die. | • Yes for biased/non-biased testing, age wafers in chambers, measure on wafer prober.<br>• Biasing of wafers, needs wafer design (DFT) to accommodate. |
| **Assembled** (with laser) full optical/electrical stressing | • Yes if laser is attached to die at wafer level.<br>• Yes for biased/non-biased testing, age wafers in chambers, measure on wafer prober.<br>• Biasing of wafers, needs wafer design (DFT) to accommodate. |
| Mechanicals: Wirebond pad integrity, laser attach integrity. | • Yes, wirebond pad to pad for testing.<br>• Yes, if laser is attached at the wafer level. |

# 6. Conclusions

- No foundry industry defined component and process PDK available but major foundries are working on making this a reality.
- All SiPh designs are unique but all have optical and electrical commonalities.
- Testing, Reliability and qualification testing falls to the end user and SiPh supplier and not the foundry (other than process tsting).
- We have presented a test plan and methodology that can be used by all industry designers and suppliers to ensure the transceiver optical modulators will meet datacom, enterprise and telecom networking reliability requirements.

# Thank You!

**For questions, please contact:**

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# Silicon Photonics Reliability and Qualification Testing - Abstract

In recent years, the optics data communications industry has leveraged mature IC CMOS tools and processes to produce Silicon Photonics (SiPh) devices. However, unlike the IC industry where multiple end-users design circuits from a common foundry defined electrical design kit following well defined design rules, no such common PDK (Process design kit) exists to date, for SiPh. Each individual end-user designs optical circuits using their own internally designed optical components (modulator diode, capacitor, Ge PD, waveguide, coupler) and lay-out design rules. This leads to a unique situation where the CMOS foundry no longer owns the reliability obligations of the components or lay-out of design. The onus for reliability and qualification now falls to the end-user, in our case MACOM. We will present how we planned our reliability testing and determined lifetime predictions of our SiPh optical components using the Form Factor Cascades-Microtech 1164 Reliability test system.