Comparative Analysis of Practical Threshold Voltage Extraction Techniques for CMOS and LDMOS Devices in 180 nm Technology

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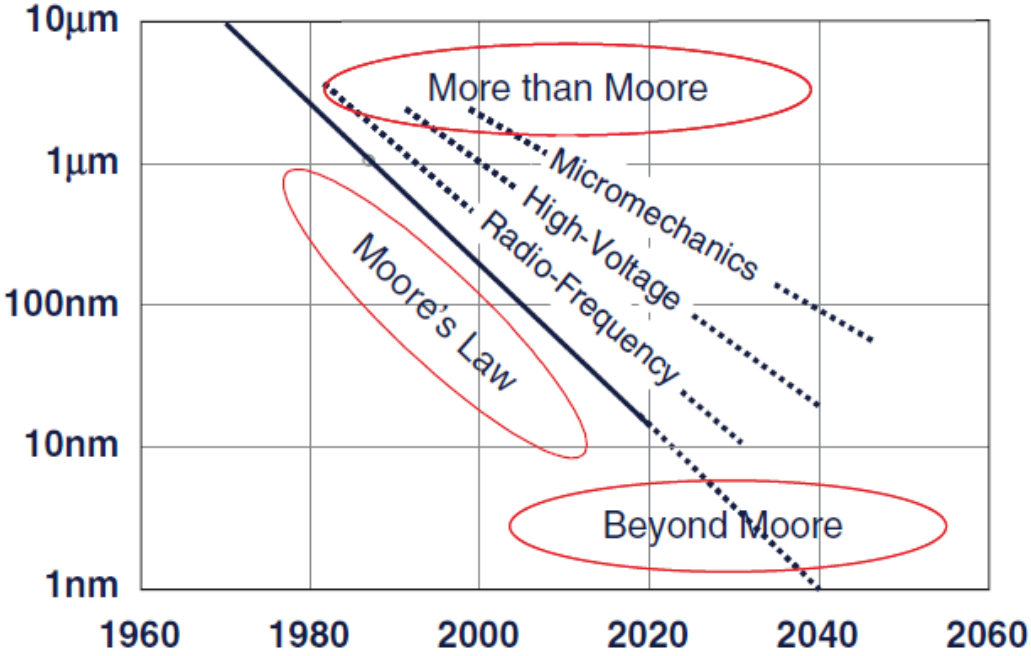
Outline

- ***Overview and Background***
- ***MOSFET Device Id-Vg Characteristics and Threshold Voltage***
- ***Threshold Voltage Extraction Techniques***
- ***Comparison of Threshold Voltage Extraction Results***
- ***Summary and Conclusion***

Overview and Background

Technology Trends : Moore's Law and More

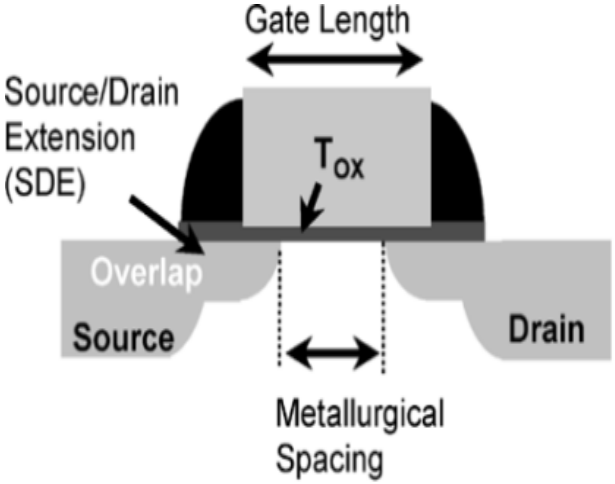


Guo Qi Zhang, Alfred Roosmalen, "The Changing Landscape of Micro/Nanoelectronics", in *More than Moore: Creating High Value Micro/Nanoelectronics*, Springer, 2009.

- **The first transistor was invented in 1947 (announced in 1948).**
- **The first IC was constructed in 1958.**
- **Gordon Moore first published his observation and prediction in 1965.**
- **It has become a self-fulfilling prophecy and a yardstick for technology progress.**
- **More-than-Moore refers to non-digital functionalities not scaling at the rate of Moore's Law.**
- **Trending: Smart manufacturing, virtual metrology, heterogeneous integration…**

MOS Scaling (Dennard Scaling)

First described by Robert Dennard *et al*. in 1974.



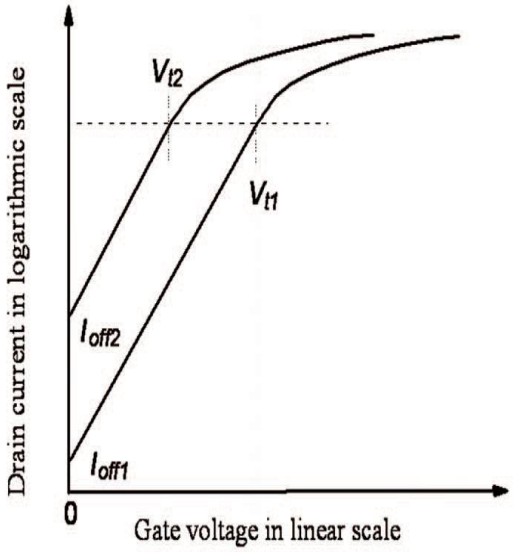
		λ=k
Dimension(linear)	λ	k
Potential	k	k
Impurity Con.	k/λ^2	1/k
Electric Field	k/λ	1
C_{ox}	λ	k
Current	k^2/λ	k
Power	k^3/λ	k^2
Power * delay	λ^2/k	k

k = voltage scale factor

λ = linear dimension scale factor

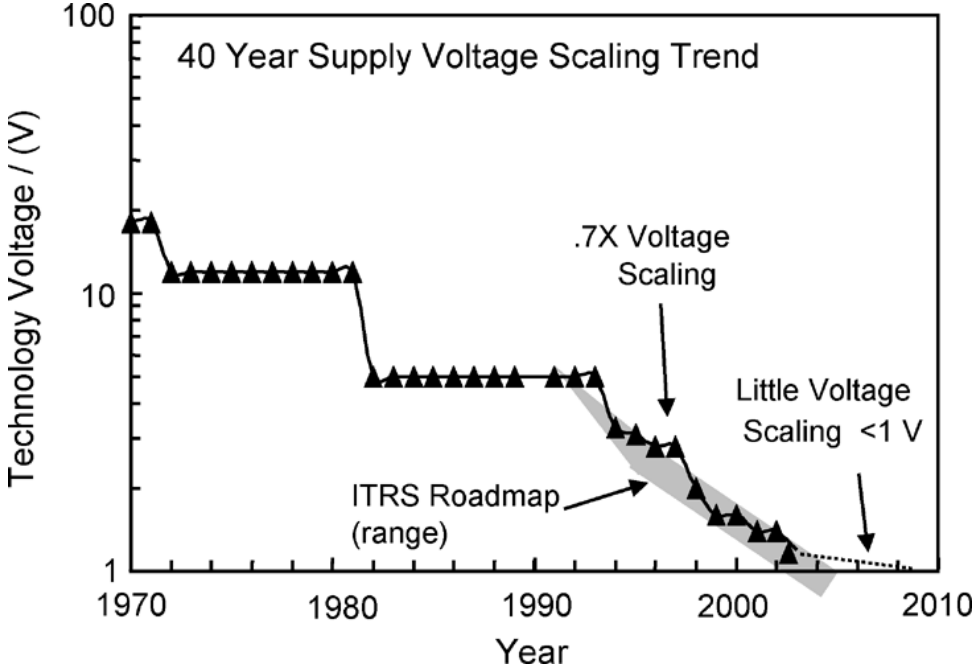
Scott E. Thompson *et al.*, IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 18, NO. 1, FEBRUARY 2005

High leakage current caused the breakdown of Dennard scaling around 2006 (Dark Silicon).

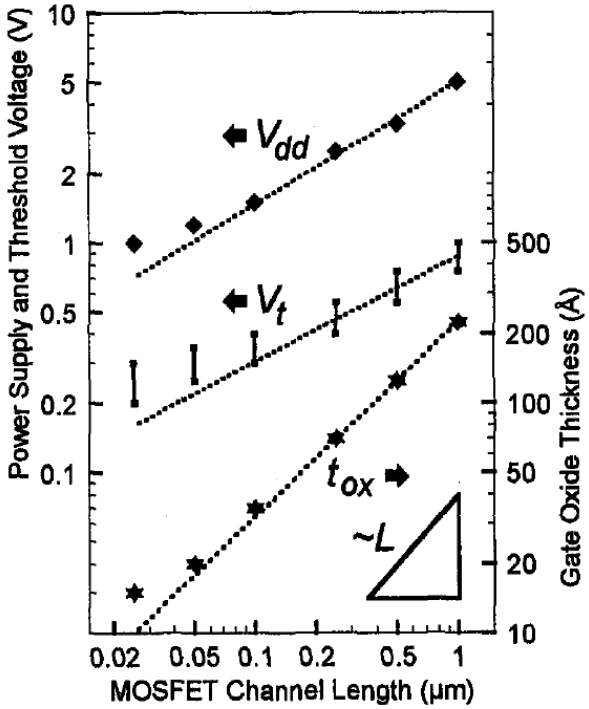


Power Supply and Threshold Voltage Scaling

V_T and V_{DD} scaling limited by off-state leakage current .

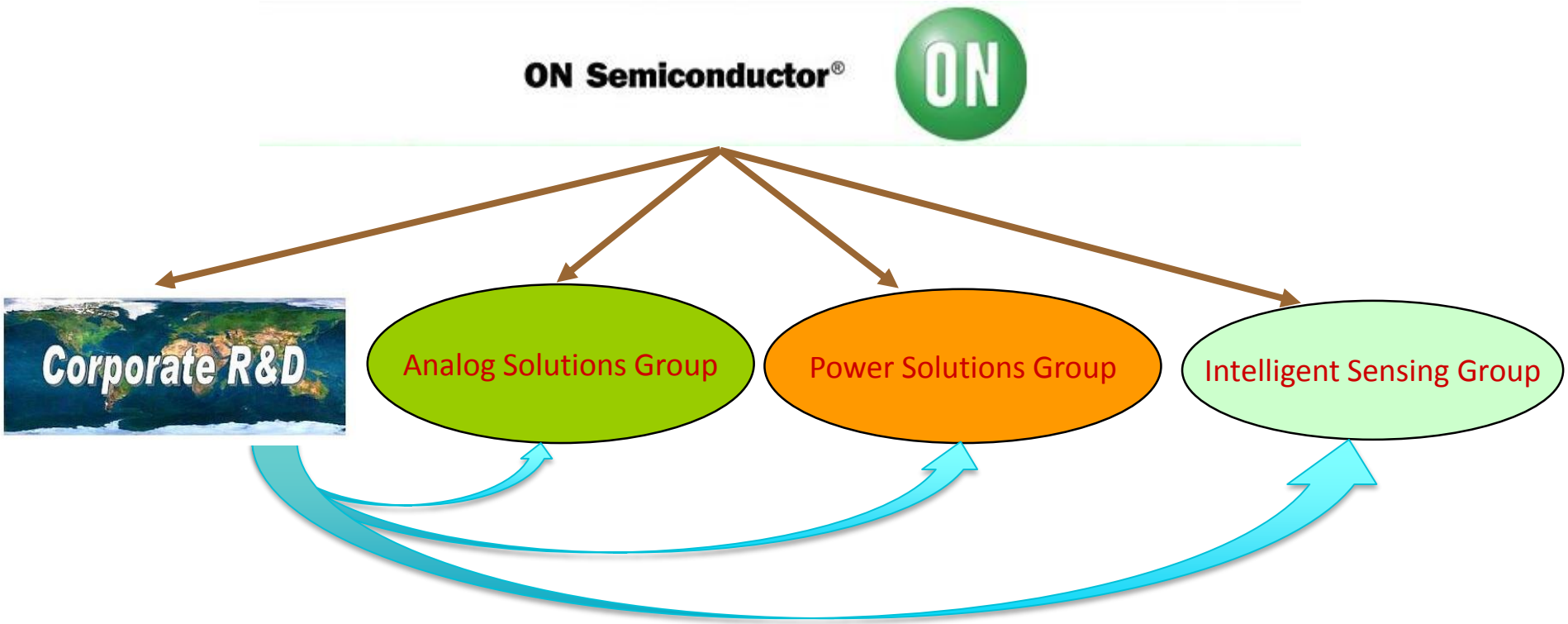


Scott E. Thompson *et al.*, IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 18, NO. 1, FEBRUARY 2005



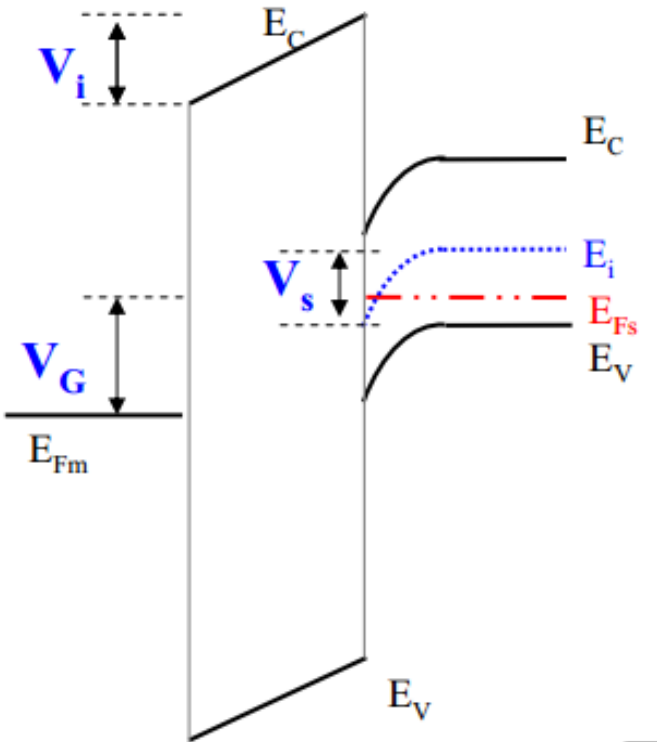
Yuan Taur, IEEE Spectrum, 1999, Vol. 36, No. 7

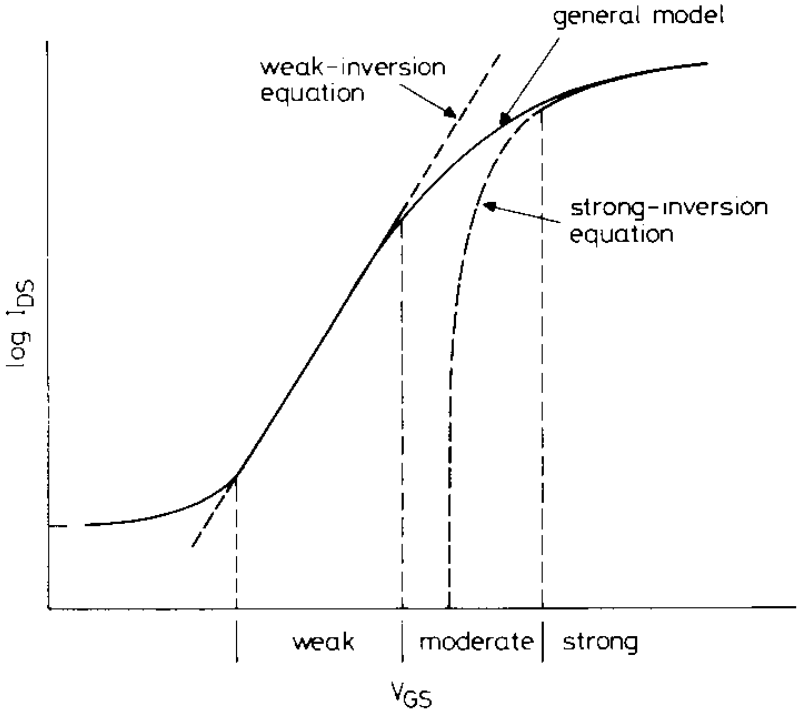
Driving Energy Efficient Innovations



MOSFET Device Id-Vg Characteristics and V_T

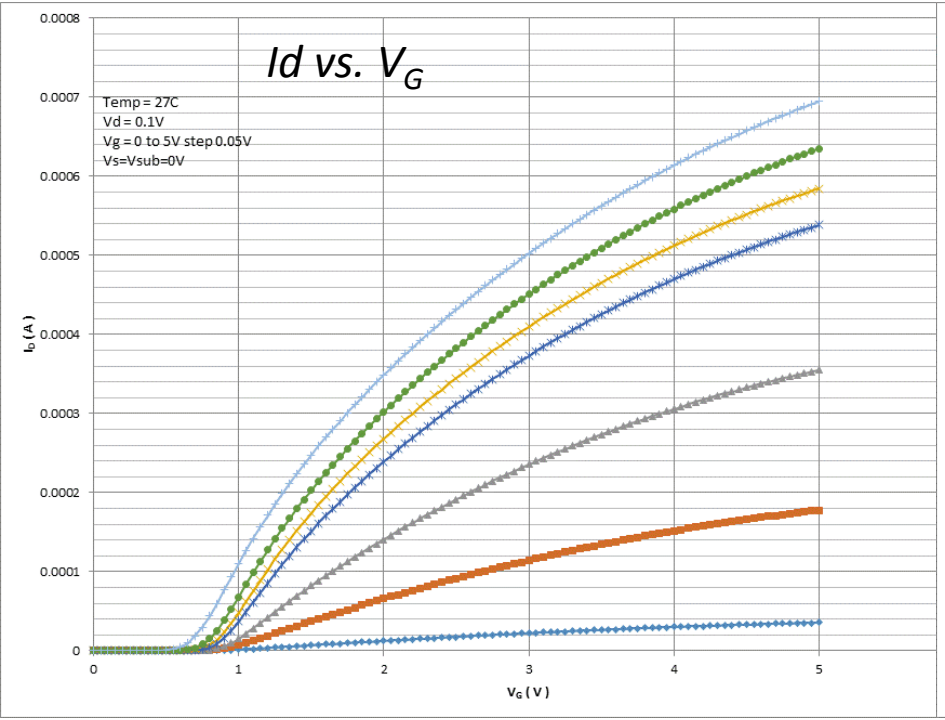
MOSFET Device Operation: Inversion Level

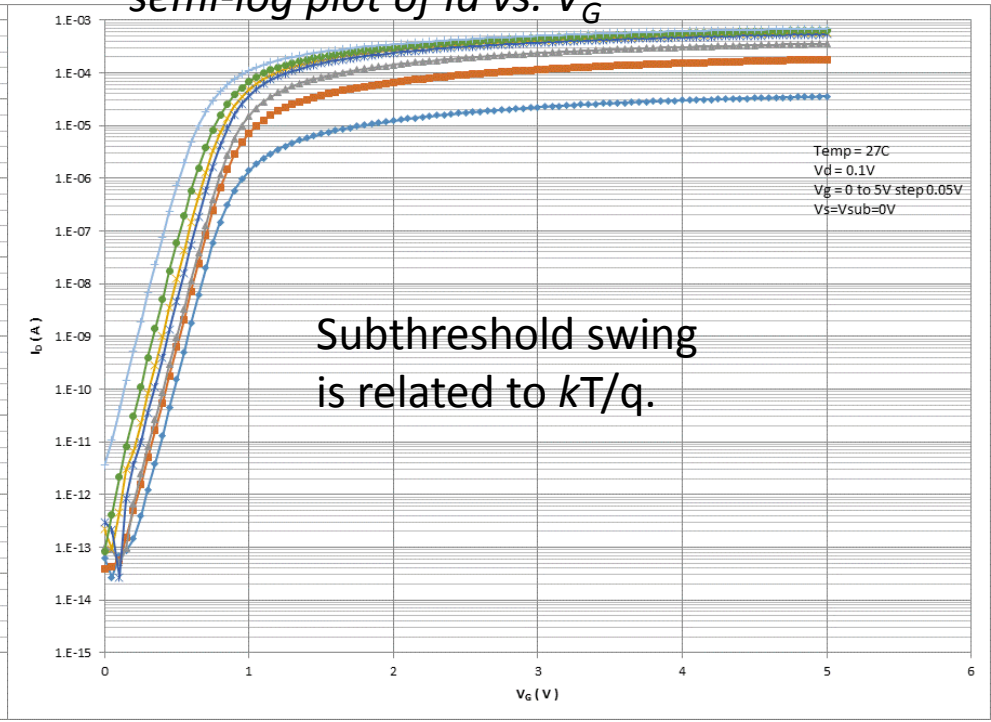




Yannis Tsividis, Operation and Modeling of the MOS Transistor, 2nd Edition, 1999

Id-Vg Characteristics of MOSFET Devices





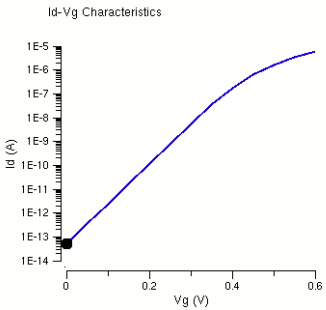
5V NMOS W = 10 µm , L = 10,2,1,0.65,0.6,0.55 0.5 µm

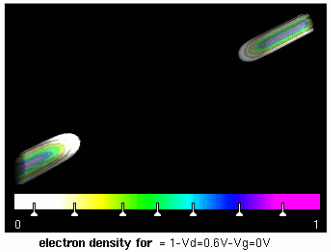
Meaning of Threshold Voltage V_T

https://en.wikipedia.org/wiki/Threshold_voltage

Threshold voltage is

- Gate voltage that turns the device "on"
  - Conceptual level, from the perspective of a user
- Minimum gate voltage required to induce the channel
  - Conceptual level, from the perspective of device physics
- Gate voltage at which strong inversion begins
  - Conceptual level, from the perspective of device physics
- Gate voltage for the inversion of surface to the same degree as the bulk (p- to n- or n- to p-)
  - Conceptual and operational level, from the perspective of device physics
    - Based on symmetry
- Gate voltage needed to reach a set value of Ids
  - Operational level, from the perspective of device characterization

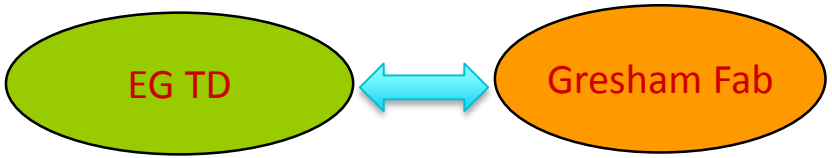




Yannis Tsividis, Operation and Modeling of the MOS Transistor, 2nd Edition, 1999

Measurement and Data Collection

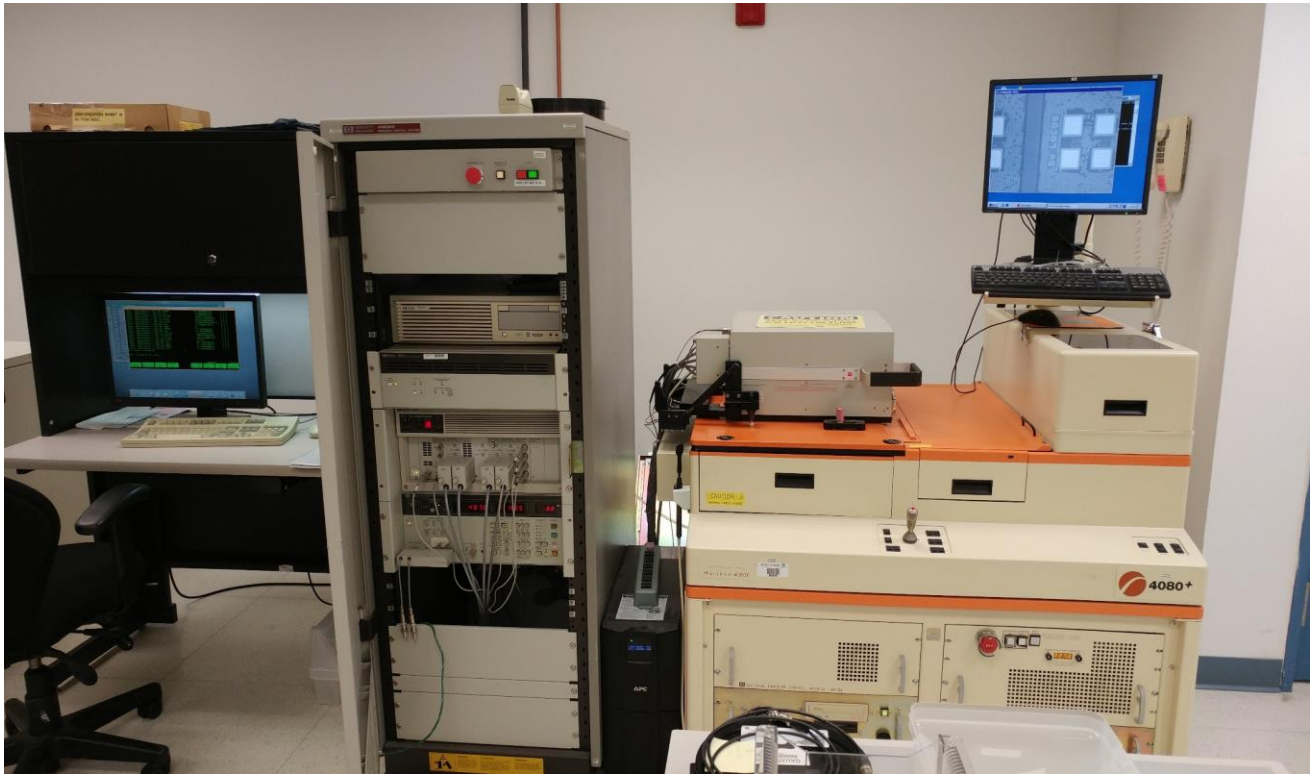
- **Process: 180 nm BCD for high power applications with high efficiency in power conversion.**
- **Gate Oxide Thickness:**
  - **2.7 nm for 1.8V MOS.**
  - **12.5 nm for 5V MOS.**
- **TCAD Simulation: East Greenwich, RI**
- **Wafer Fab: Gresham, OR**
- **Device Evaluation: East Greenwich, RI**



Test Equipment in the Lab

- Agilent 4156C, 41501B Expander Box, E5250A Switch Matrix
- Cascade 12K Semi-Automatic probe station
- Temptronic Temp controller TP 03000, -50C to 200C.
- Metrics IC/V software package.

Test Equipment in the Lab



- HP4062 Parametric Test System (Agilent 4142 SMU)
- Electroglas 4080+ Prober
- Chuck Temp 25C to 130C.
- HP BASIC programming language

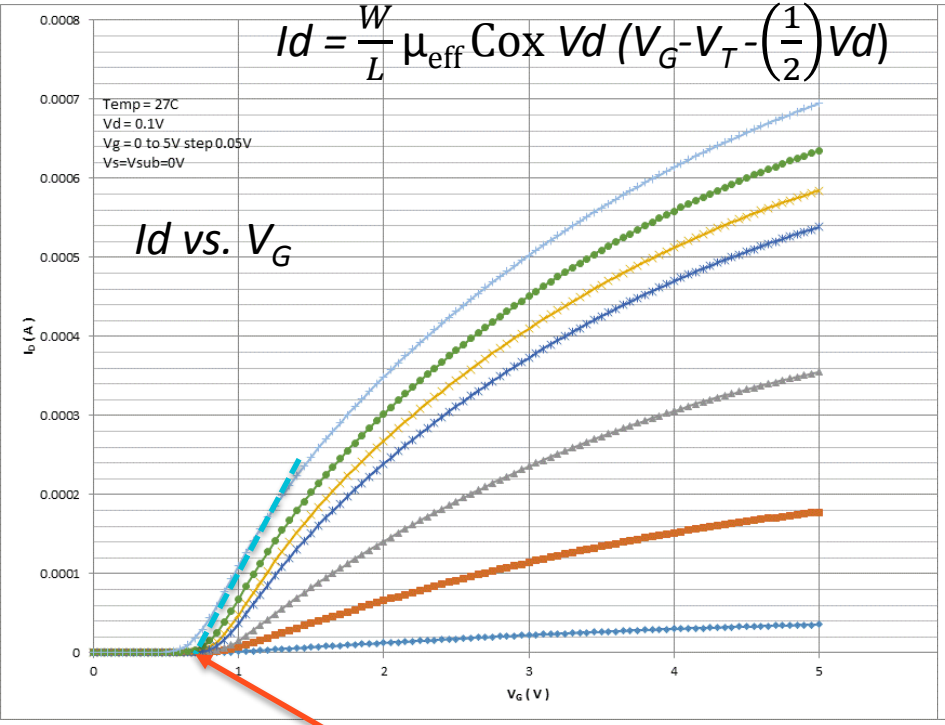
Threshold Voltage Extraction Techniques

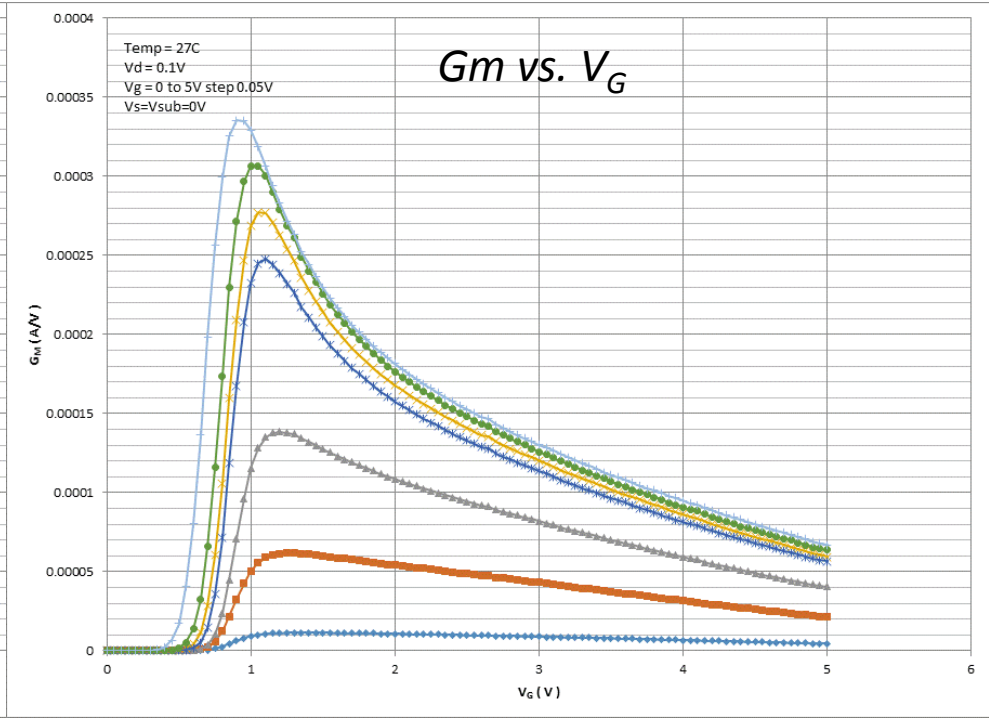
Threshold Voltage Extraction Techniques

- Point of Maximum Slope in Id-Vg Curve (from strong inversion)
  - Extrapolation of the Id-Vg curve from maximum gm in the linear region (LEID).
- Ratio Method: Y-Function (from strong inversion)
  - Extrapolation of Id/$\sqrt{\mathrm{gm}}$ in the linear region. This method is considered to be unaffected by mobility degradation and series resistance effects.
- Subthreshold slope and pre-defined current (from weak inversion)
  - Extrapolation from the subthreshold region to a pre-defined current using subthreshold slope.
- Constant Current
  - Usually scaled by width and length in the form of Id0 x (W/L) with Id0 dependent on technology and specific device type.
- Transition Method (transition from weak to moderate and strong inversion)
  - Integration-based: Construct an auxiliary function $G1(Vg, Id) = Vg - \left(\frac{2}{Id}\right) \int_0^{Vg} Id\, dVg$.
  - G1 is zero if Id is linear with Vg (a measure of nonlinearity).
  - With the transition of Id between diffusion current and drift current, the maximum value of G1 gives V_T .

Illustration of V_T Extraction from Maximum Slope (Gm)

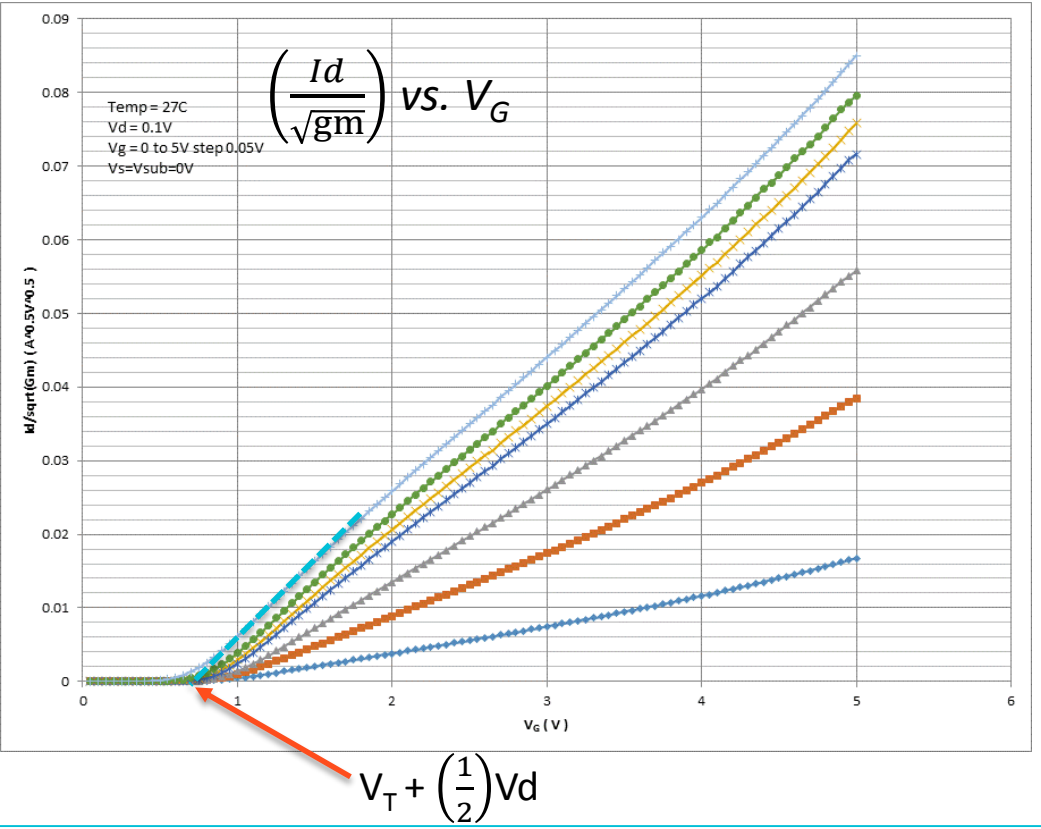
$$Id = \frac{W}{L}\mu_{eff}\,Cox\,Vd\,(V_G - V_T - \left(\frac{1}{2}\right)Vd)$$





$$V_T + \left(\frac{1}{2}\right)Vd$$

Illustration of V_T Extraction from Ratio ($Id/\sqrt{gm}$) Method



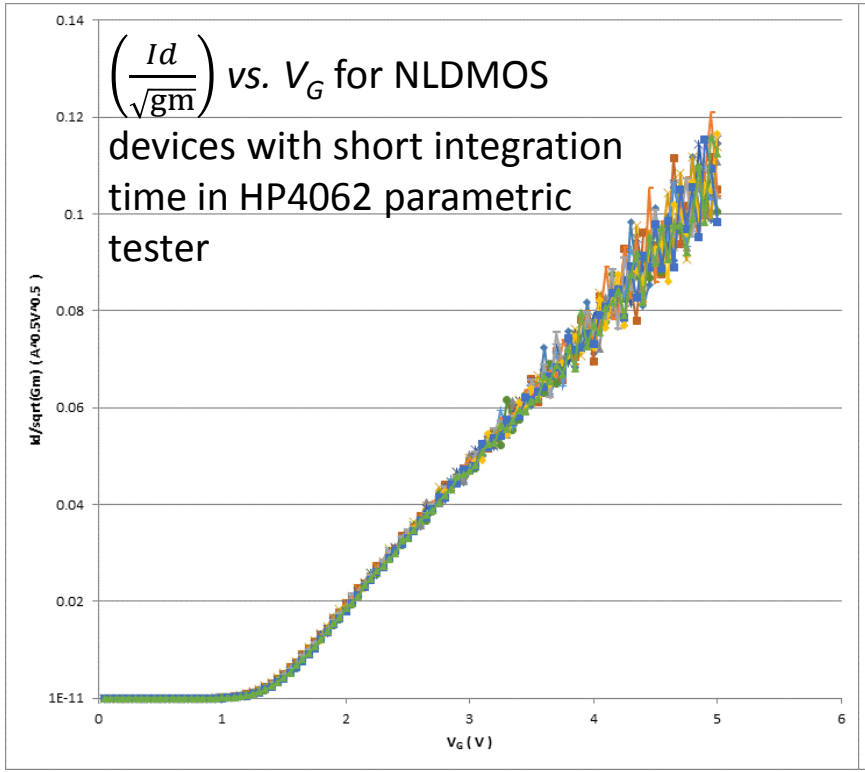
Consider R_{SD} and μ_{eff} in Id expression, and obtain

$$\left(\frac{Id}{\sqrt{gm}}\right) = \sqrt{k_0 Vd}\,\left(V_G - V_T - \left(\frac{1}{2}\right)Vd\right)$$

independent of R_{SD} and μ_{eff}

where $k_0 = \left(\frac{W_{eff}}{L_{eff}}\right)\mu_0 Cox$

Noise Effect in Id/$\sqrt{gm}$ Ratio Method



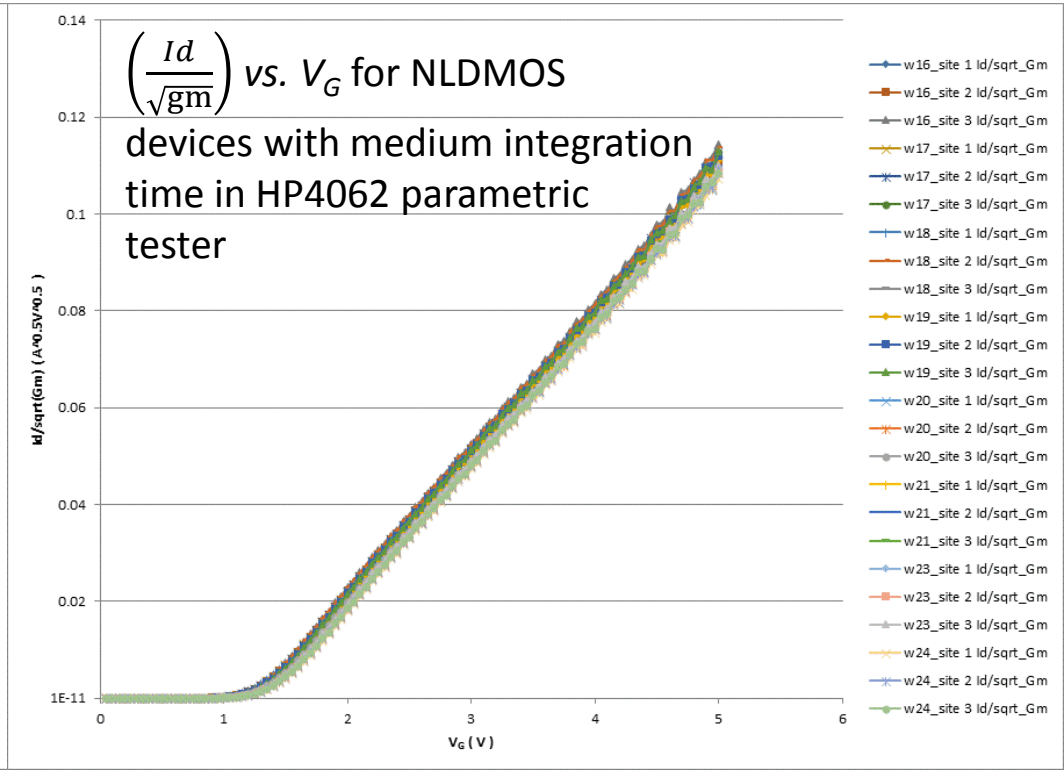


Illustration of V_T Extraction from Constant Current

The choice of Id0:

Id = Id0 x (W/L)

- Many use Id0 = 100nA.
- Id0 can be selected from LEID method:
  - Id0= (Id at V_T) / (W/L)
- In this way, Id0 is not set arbitrarily, and becomes a Technology-Specific Scaled Current (TSSC).

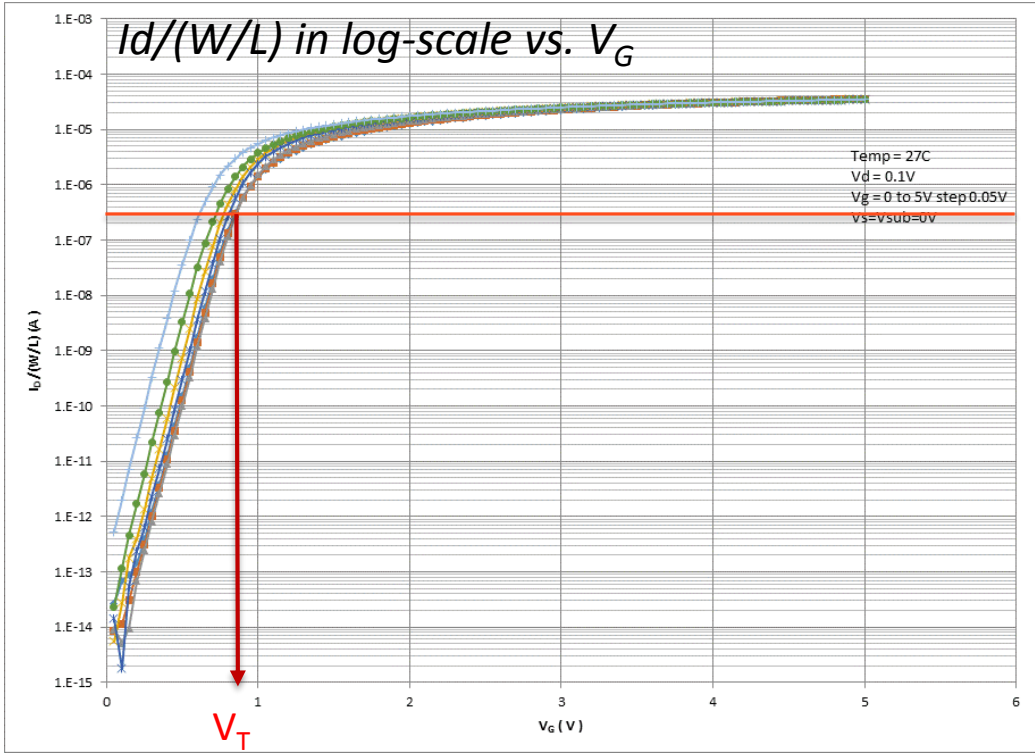
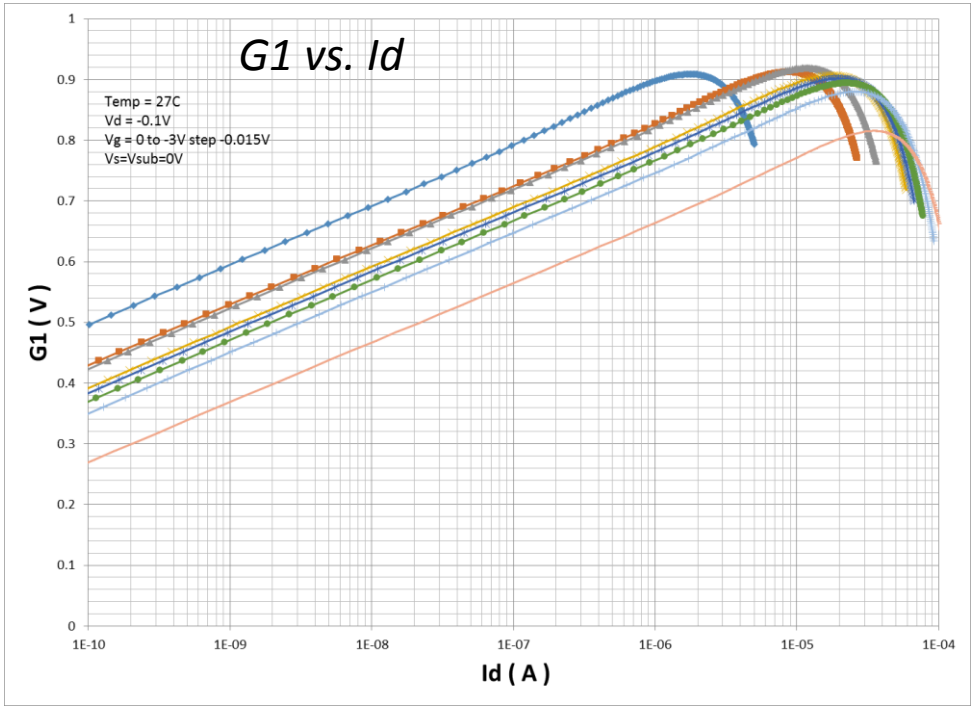


Illustration of V_T Extraction from Transition Method



Construct $G1(Vg, Id) = Vg - \left(\frac{2}{Id}\right) \int_0^{Vg} Id \, dVg$

Id is composed of diffusion current and drift current with different dependencies on Vg.

With the transition of Id from weak to moderate and strong inversion, maximum value of G1 gives V_T.

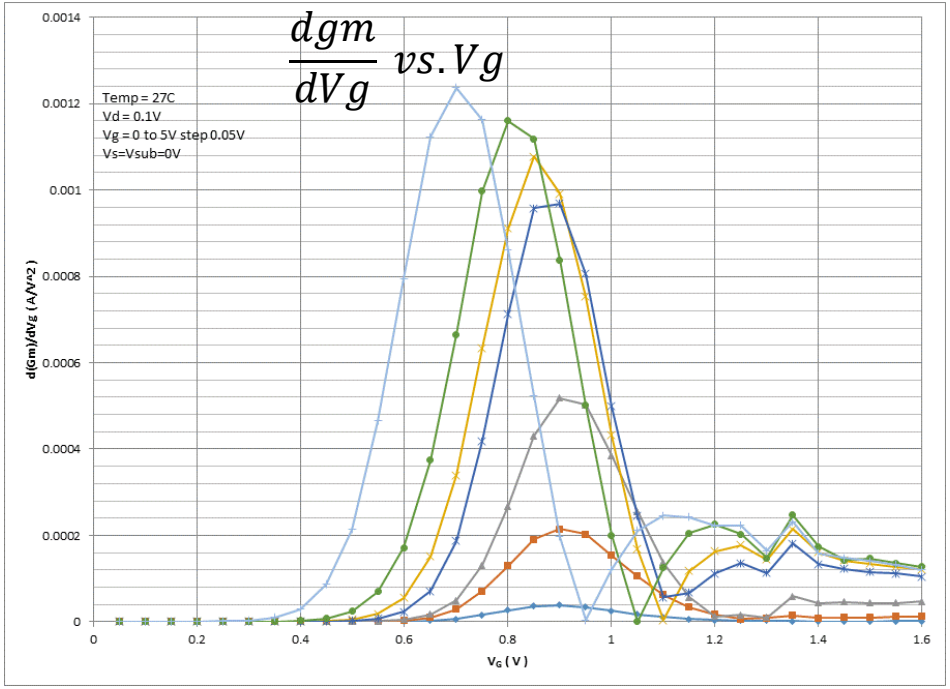
Integration-based extraction methods present no noise issue as seen in the graph on left.

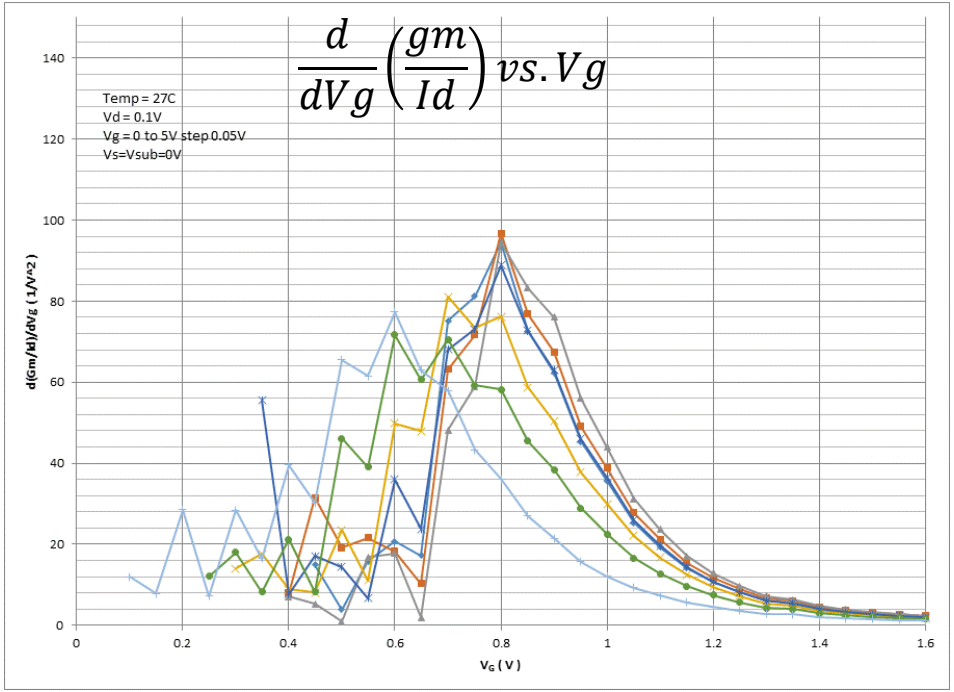
5V PMOS W = 10 µm , L = 10,2,1.5,1,0.9,0.8,0.7,0.55 µm

More Threshold Voltage Extraction Methods

- Second Derivative (Transconductance Change)
  - Vg at which second derivative of Id vs. Vg (or dGm/dVg) assumes its maximum.
  - Is Dirac Delta function in Level 1 SPICE model: Id=0 for Vg<Vt, Id linear with Vg for Vg>V_T .
  - Data could be noisy with two derivatives.
- gm/Id method with its maximum derivative to Vg (from gm/Id methodology)
  - Analytical modeling relates this to charge in inversion layer and it occurs when gm/Id drops to $\frac{2}{3}$ of its maximum value when Vd approaches zero, and 0.72 of its maximum value when Vd ≥ 3~ 4(kT/q).
- gm/Id method with the equality of diffusion current and drift current (from gm/Id methodology)
  - Shown by analytical modeling to occur when gm/Id drops to $\frac{1}{2}$ of its maximum when Vd is small
- Point of Maximum Slope in Gm-Vg Curve (Not covered in this study)
  - Extrapolation of the Gm-Vg curve from maximum dGm/dVg in the linear region.
- Model-based Methods (Not covered in this study)
  - Adjusted Constant Current (ACC), Quasi-Constant Current (QCC), etc.

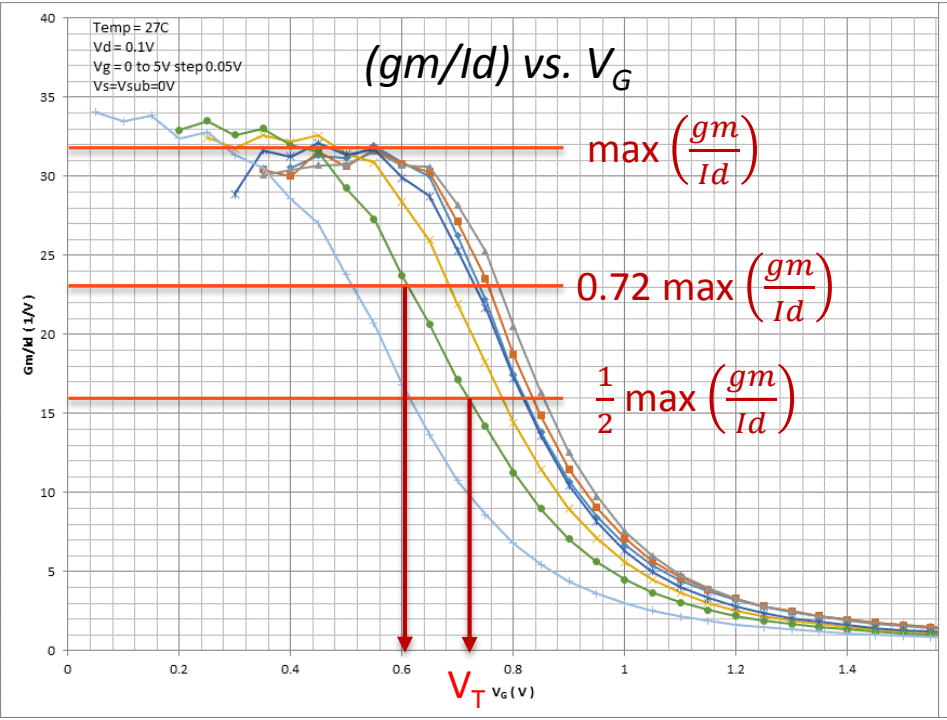
Illustration of V_T Extraction with Second Derivative

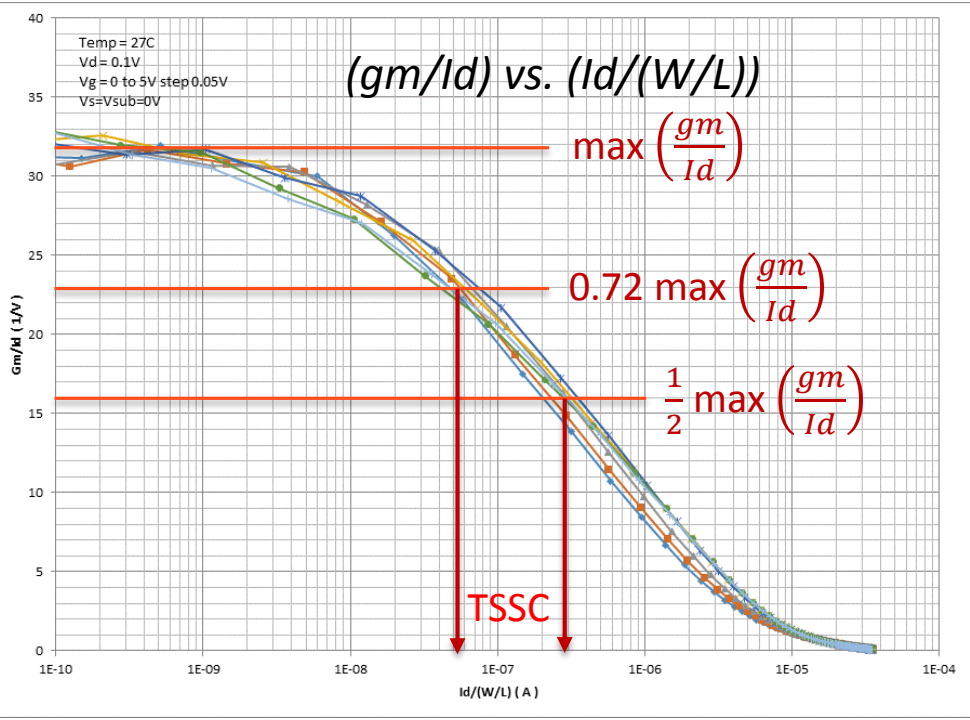




Resolution of V_T extraction is limited by Vg step size

Illustration of V_T Extraction from gm/Id Method





Gm/Id curve covers device operation from weak to moderate and strong inversion.

Comparison of V_T Extraction Results

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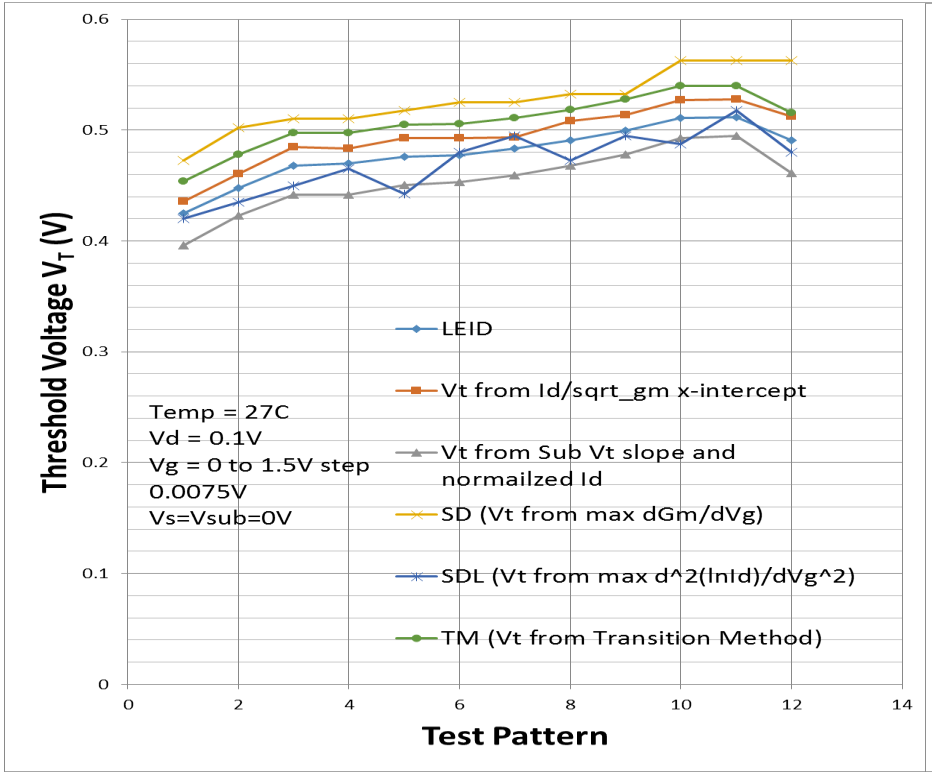
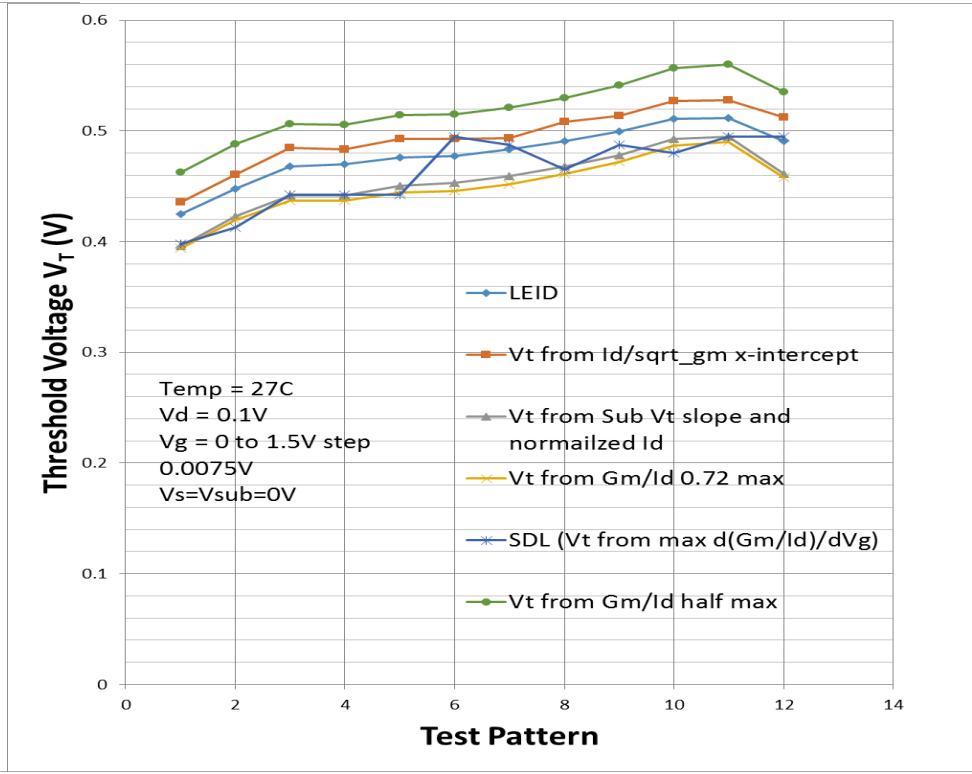
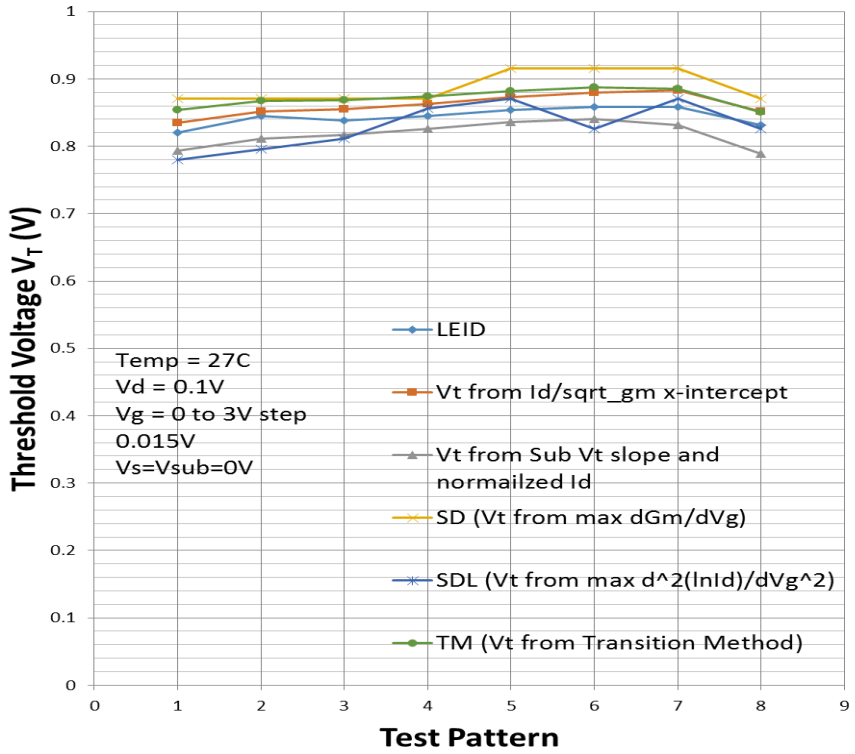


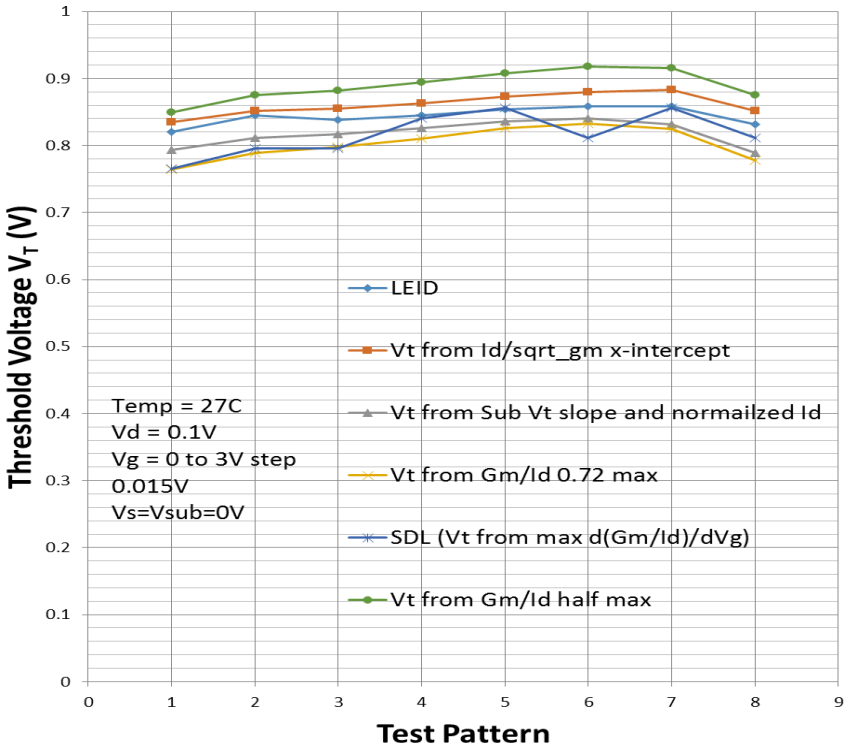


1.8V NMOS W = 10 µm with varying channel lengths.

Id0 = 400nA. Vg step size 7.5mV

Comparison of V_T Extraction Results

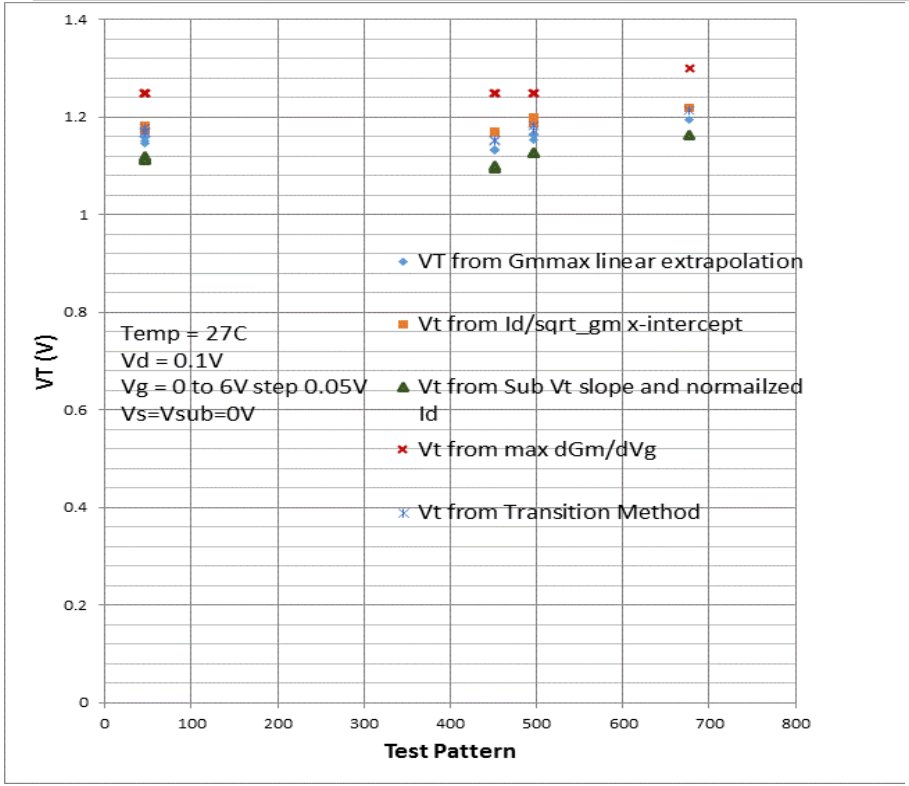


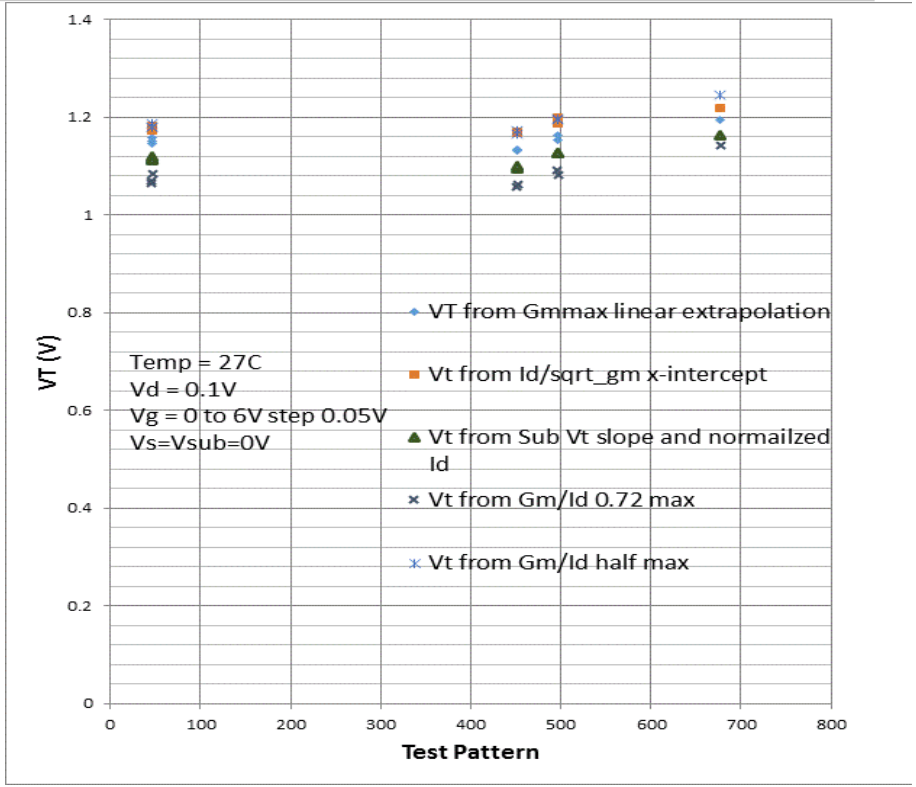


5V NMOS W = 10 µm with varying channel lengths.

Id0 = 300nA. Vg step size 15mV

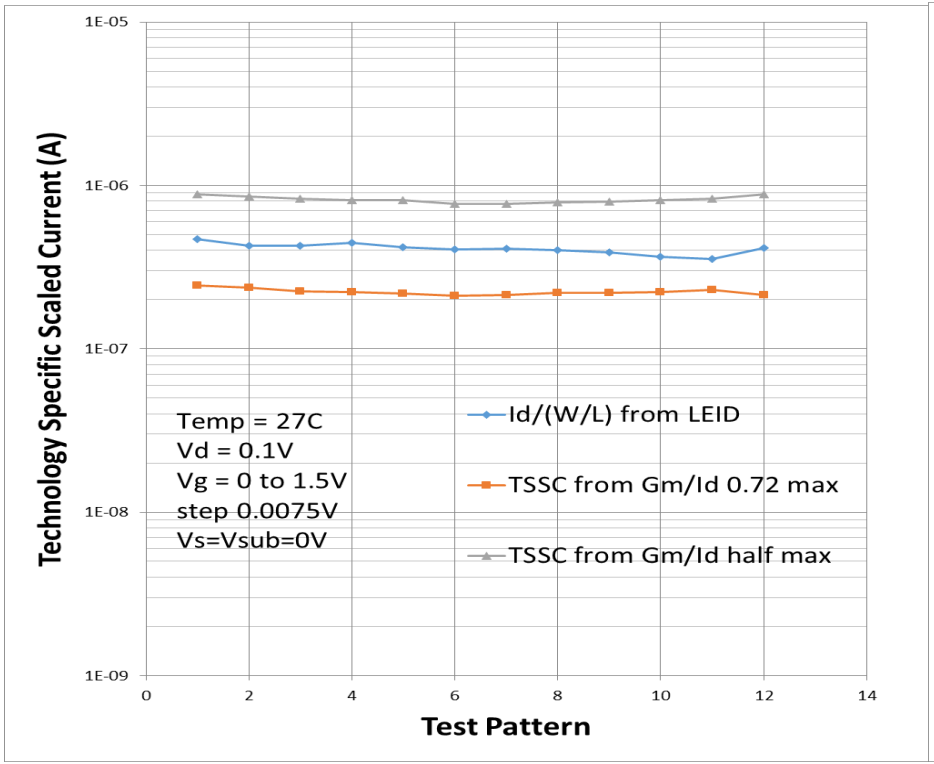
Comparison of V_T Extraction Results for LDMOS



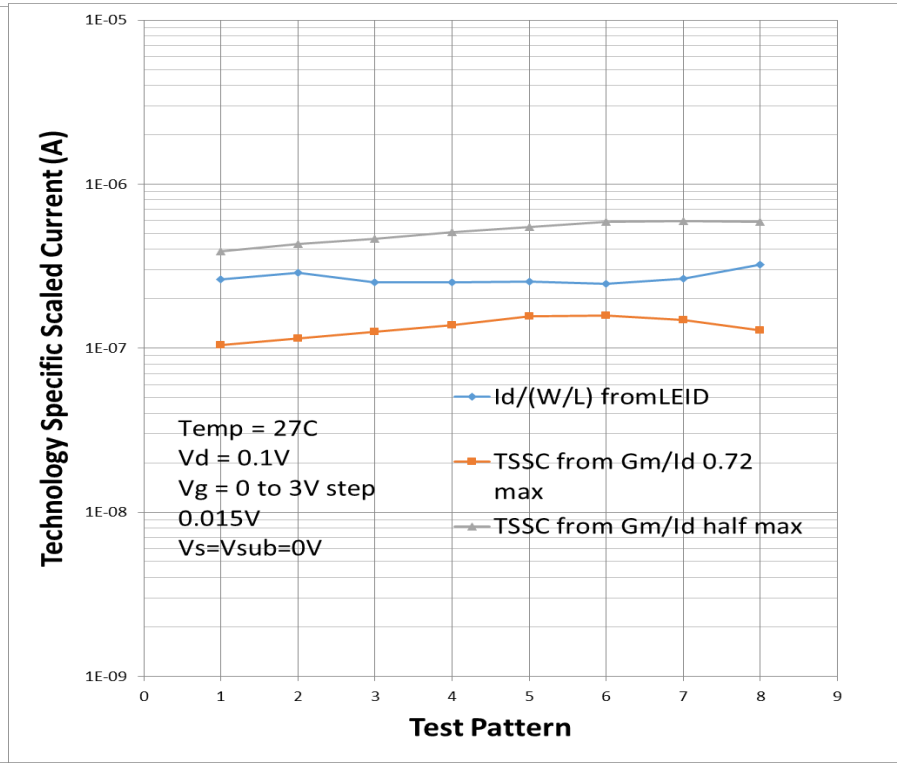


45V NLDMOS Id0 = 100nA. Vg step size 50mV

Comparison of Technology-Specific Scaled Current



1.8V NMOS W = 10 µm with varying channel lengths.



5V NMOS W = 10 µm with varying channel lengths.

Discussion of V_T Extraction Results

- $Id/\sqrt{gm}$ ratio (Y-Function) method and transition method both produce V_T extraction results in good agreement with V_T from LEID method (slightly higher).
- V_T extraction results from subthreshold slope and pre-defined Id is consistent with V_T from LEID method (slightly lower). This method is valid only when there is no deviation of subthreshold Id-Vg characteristics from a straight line in semi-log plot (so is the Match Point method in literature).
- Technology-Specific Scaled Current (TSSC) can be selected from Id at V_T from LEID method for each device category (e.g., 1.8V NMOS, 5V NMOS or 45V NLDMOS).
- Second derivative method produces V_T extraction results higher than V_T from LEID method.
- Gm/Id curve covers device operation from weak to moderate and strong inversion. V_T from LEID method lies between the two predictions from gm/Id methodology.

Comparison of V_T Extraction Methods

Extraction Method	Speed	Noise	Faithfulness	Notes
LEID	Slow	Medium	High	Common practice
Ratio Method	Slow	Medium	High	
Subthreshold Slope and pre-defined current	Medium	Low	Medium	Requires “calibration”
TSSC	Fast	Low	High	Requires “calibration”
Transition Method	Medium	Low	High	
Second Derivative	Slow	High	Medium	
0.72 (Gm/Id) max	Medium	Medium	Medium	
0.5 (Gm/Id) max	Medium	Medium	Medium	

Summary and Conclusion

Summary

- ***Aggressive threshold voltage (V_T) scaling faces challenge on energy efficiency since V_T is related to OFF state leakage current.***
- ***There is no single definition of threshold voltage, and many extraction techniques exist for this key device parameter.***
- ***Practical threshold voltage extraction techniques tend to avoid noise caused by performing second (or even third) derivative.***
- ***Several extraction methods produce results close to V_T from LEID method, and TSSC can be selected from LEID method.***

Test Insights from Lab to Fab

Technology-Specific Scaled Current (TSSC)

Id = Id0 x (W/L)

- Id0 can be selected from LEID method:
  - Id0= (Id at V_T) / (W/L)
- Id0 is Technology-Specific Scaled Current (TSSC) that applies to all geometries of the same device category.
- Id0 information can be used to monitor V_T shift in reliability tests.
- Id0 information can be provided from lab to fab to save time on V_T measurements.

Acknowledgment

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Thank You!

For questions, please contact:

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