Optimized Test Sequence Methodology for Minimal Test Time and Maximal Throughput

Liang Yuan Dai*, Yu-Han Hung, Robert Polster, and Keren Bergman

Lightwave Research Lab, Columbia University

****LD2719@columbia.edu***

COMPASS 2018

Testing in Silicon Photonics

The Complexity of Light Testing/Coupling

Datacom

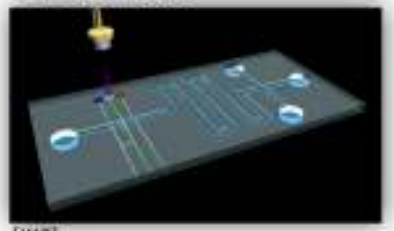
[AIST]

- High Port Count

Transceiver

- RF Electronics

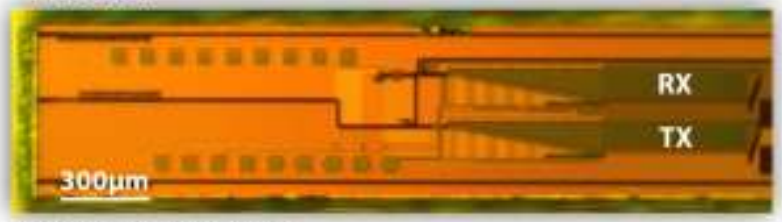
Biosensor



[KIT]

- Microfluidics Layer

LIDAR



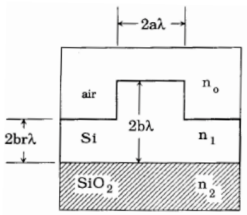
[MIT Christopher V. Poulton]

- Micro-antenna Array

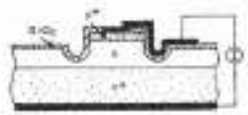
Silicon Photonics Technology

Fundamental Discoveries

- low-loss, single-mode waveguiding

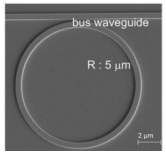


- optical coupling
- optical modulation via carrier injection

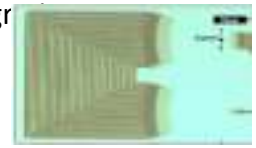


Introduction of Innovative Devices

- microring resonators



- arrayed waveguide gr



- high-speed MZM modulators and switches
- germanium photodetectors
- ultra low-loss waveguides
-

Integration and Commercialization

Hybrid platforms

Monolithic CMOS Integration

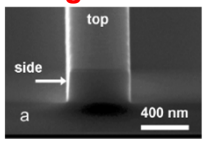
Transceivers for Datacom

Academic Foundry Services

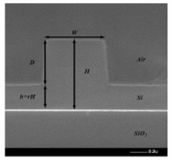
1990 — 2000 — 2010 - present

Silicon photonics basic components

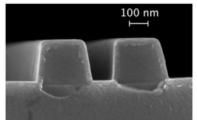
Waveguides



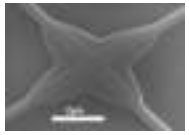
Strip waveguide (IBM)



Rib waveguide (Surrey, UK)



Slot waveguide (Aalto University, Finland / Karlsruhe Institute of Technology, Germany)



Rib waveguide crossing (IMEC, Belgium)

Laser Sources

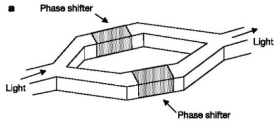
On-chip WDM laser Source (Aurrion)

Modulators

Microring modulator (Cornell)

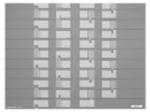
Electro absorption modulator (Kotura/Oracle)

Microdisk modulator (MIT)



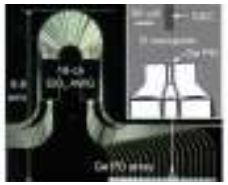
Mach-Zehnder modulator (Intel)

Photodetectors

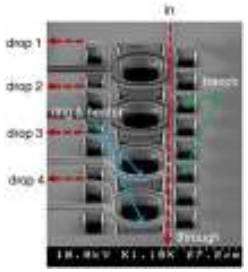


Ge Photodetector (Aurrion)

WDM mux/demux



Arrayed-waveguide-grating (AWG) filter (NTT, Japan)



Demux. filter (Kotura/Oracle)

Switches

Mach-Zehnder switch (IBM)

Microring switch (Cornell)

Silicon Photonic Optical I/O

Main impediments of electronic I/O

Bandwidth density at the pin level

Bandwidth-limited transmission channels (RC constants)

- Limited data rates per pin
- Poor scaling with distance

Optical I/O Requirements

Improve BW density

Low packaging cost

} ⟹ **WDM operation required**

Power efficiency competitive with electronics – difficult (at short distances)

Dense scalable integration of many devices (small footprint)

Drivers of Silicon Photonics

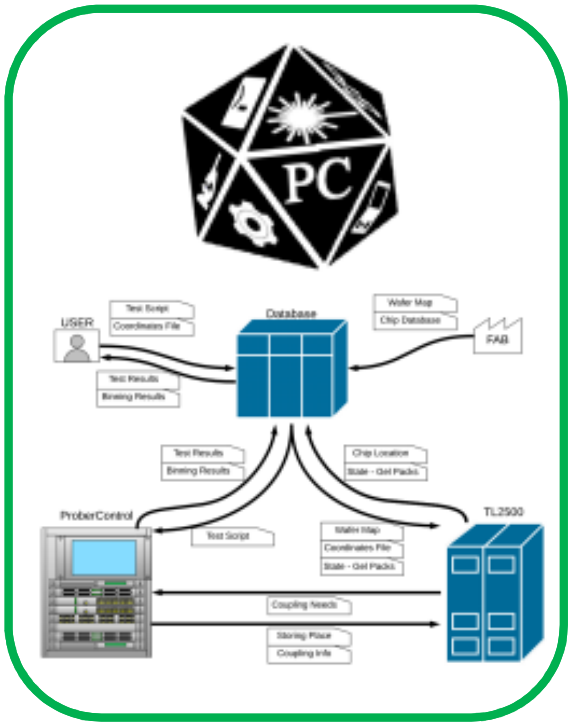
- Silicon photonics arrives in the marketplace
- Large Demand, Low Supply
- Supply limited due to bottlenecks in testing, not fabrication [1]

[1] Poister, R., et al. (2018). Challenges and solutions for high-volume testing of silicon photonics. Silicon Photonics XIII. doi:10.1117/12.2292235

Motivation

Hardware

Control Software



Next Step: Deciding How to Test

Motivation

Tools

[Roos Instruments] [Tokyo Electron]

$ 2,000,000
(5 year lifetime)

Cost of Ownership

[Modular Cleanrooms]

$ 100,000 p.a.
(30% of procurement costs)

3 cent per second[1]

vs

10 - 30 cents for 10 mm^2 of chip area

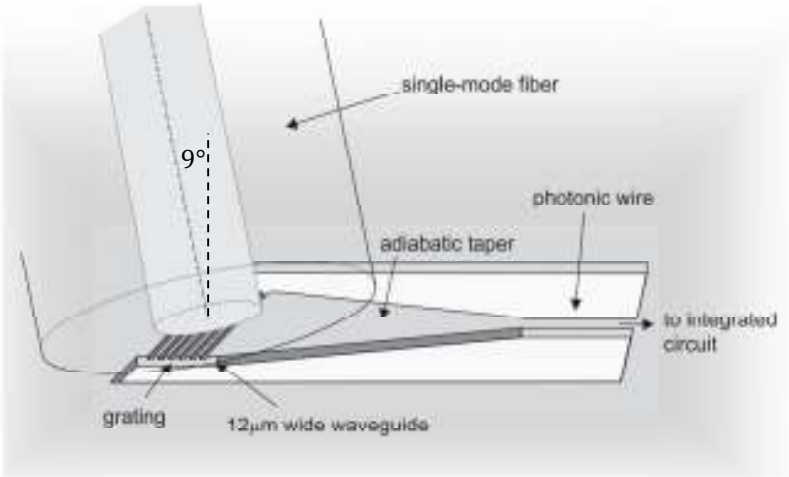
Staff

$ 300,000 p.a.

Minimize Total Test Time to Reduce Overall Cost and Improve Overall Throughput

The Complexity of Light Coupling

Photonic Coupling



- Probe cannot touch coupler
- Extremely sensitive to alignment mismatch

Electrical Coupling

[MPI]

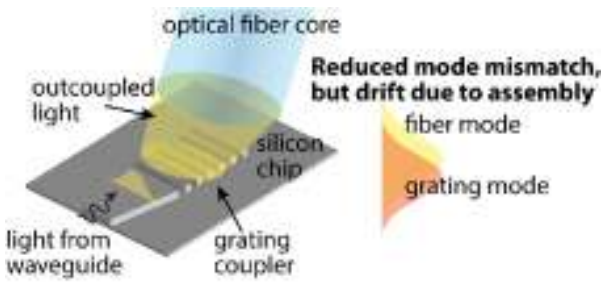
- Probe needs to contact the electrical pads
- Signal fidelity not dependent on placement of probe on pads

Review of Current Coupling Schemes

Grating Couplers:

Advantages:
- Reduced mode mismatch
- Accessible on wafer scale

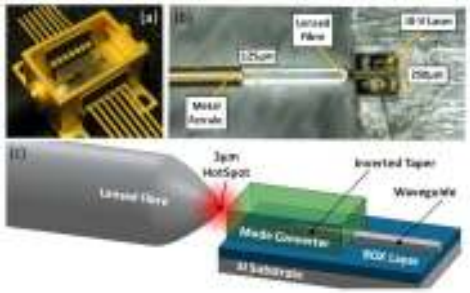
Disadvantages:
- High polarization dependent loss
- Low optical bandwidth
- Higher insertion loss



Edge Couplers:

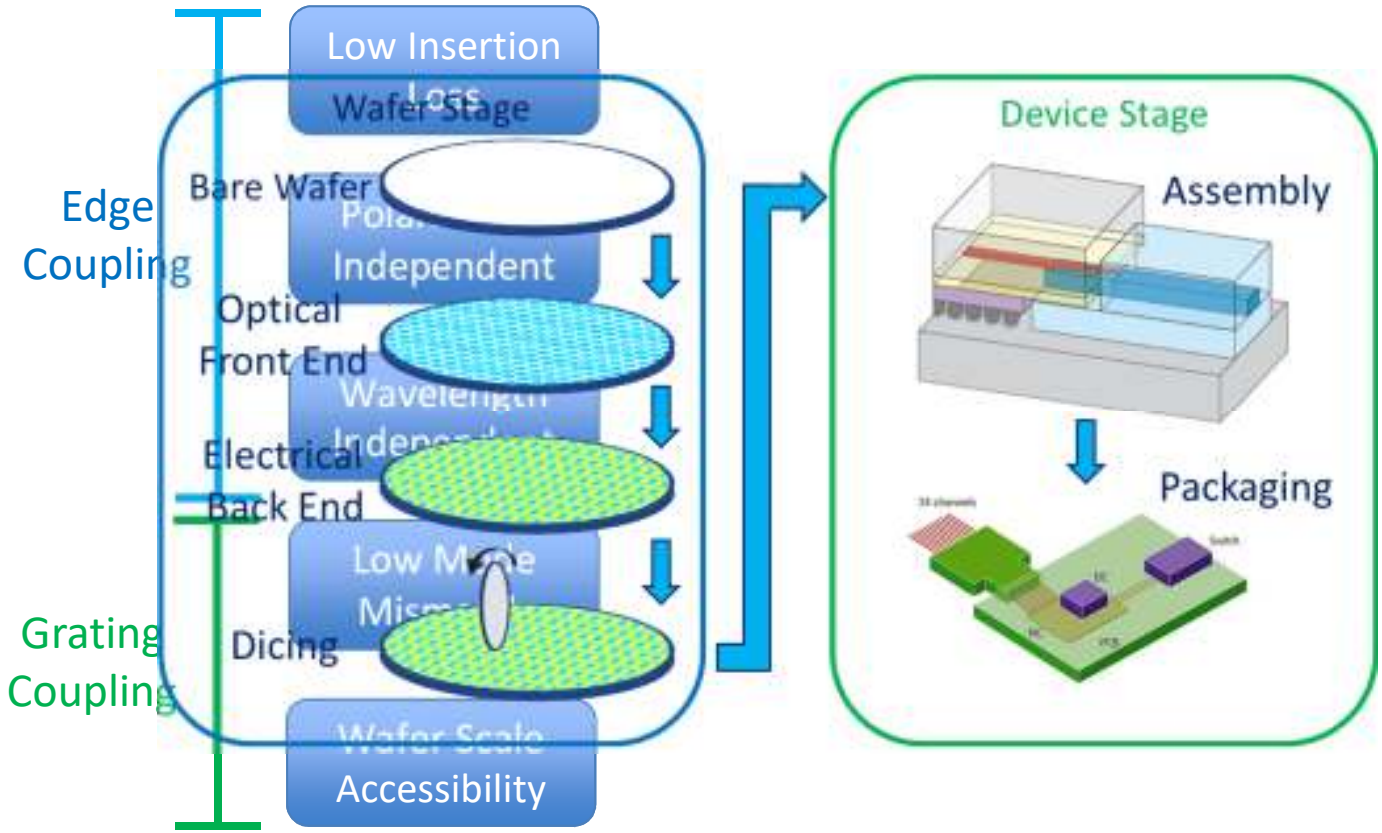
Advantages:
- Lower insertion loss
- High optical bandwidth
- Low polarization dependent loss

Disadvantages:
- Not easily accessible on wafer scale
- Large mode mismatch

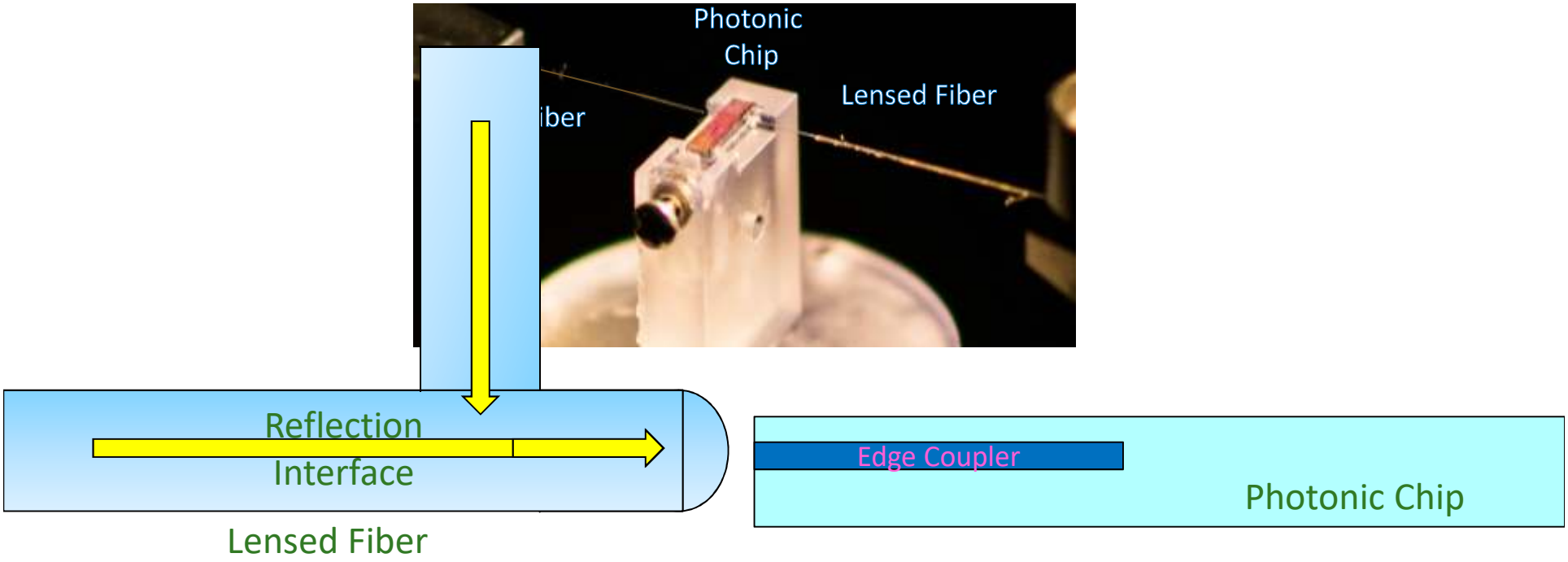


[Tyndall]

Ideal Coupling Characteristics and Wafer-Scale Test



Accessible Edge Couplers



Lateral View of Edge Coupling

Summary

Grating Coupling:

Advantages:
- Reduced Mode Mismatch
- Accessible on wafer scale

+

Lateral Edge Coupling:

Advantages:
- Low insertion loss
- High optical bandwidth
- Low polarization dependent loss

=

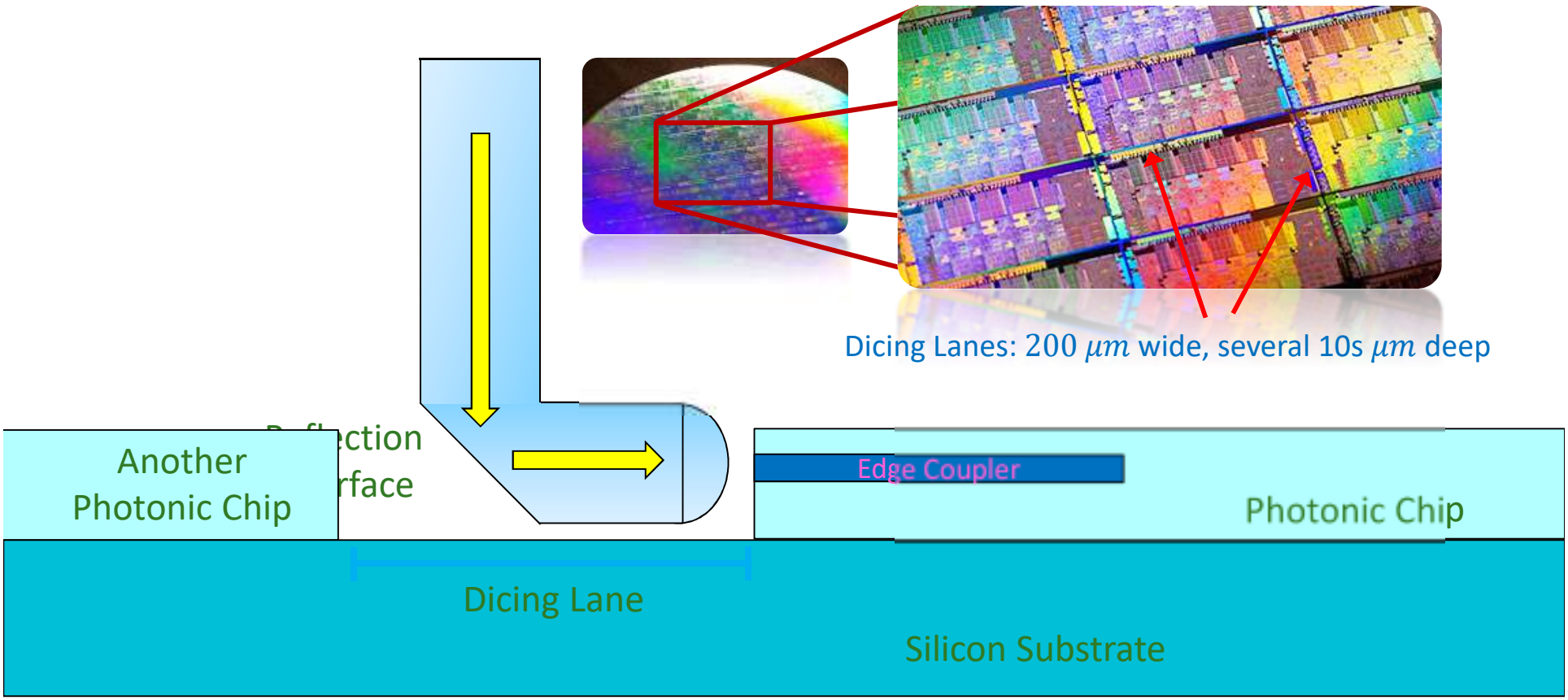
Vertical Edge Coupling:

Advantages:
- Reduced Mode Mismatch
- Accessible on wafer scale
- Low insertion loss
- High optical bandwidth
- Low polarization dependent loss

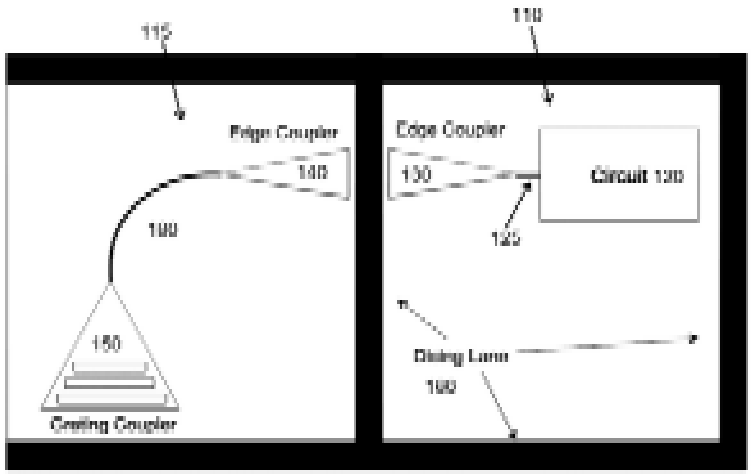
Additional Highlights

- Capable of performing high-throughput testing on wafer scale
- Requires no extra device area or change to fabrication process

Dicing Lanes



Coupling Solutions

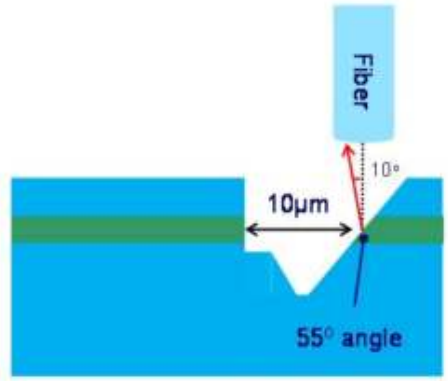


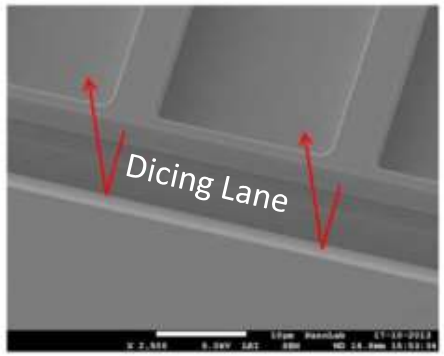
Edge to Edge Coupling [1]:

- allows to test final product
  - extra costs

Optical fiber probe [2]:

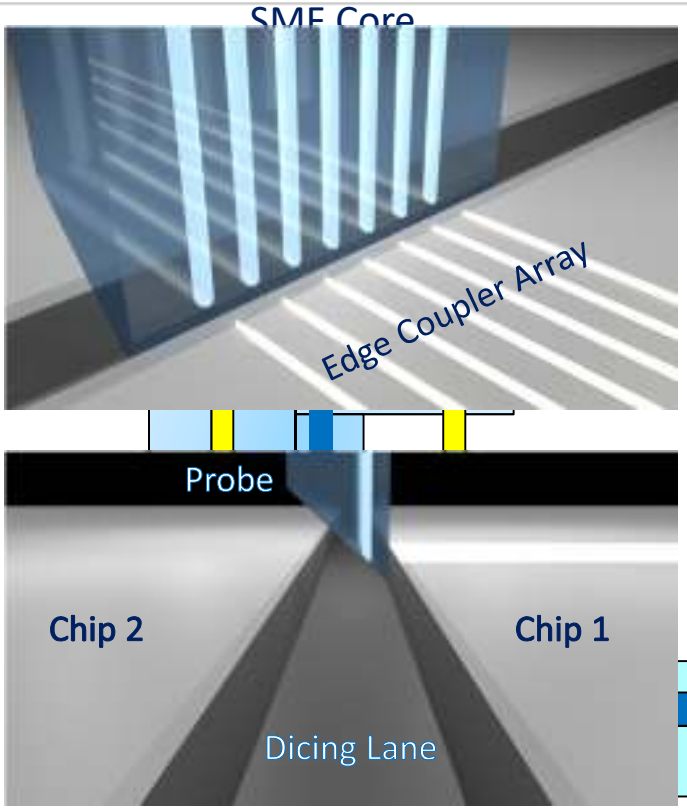
- allows to test final product
  - needs to be developed for Si Photonics





1. Novack A, et al "Test systems and methods for chips in wafer scale photonic systems." United States patent application US 14/860,537. (2015).
2. Santos R, et al "Vertical coupling mirror for on-wafer optical probing of photonic integrated circuits." Integrated Photonics Research, Silicon and Nanophotonics, pp. IM3A-3 (2014).

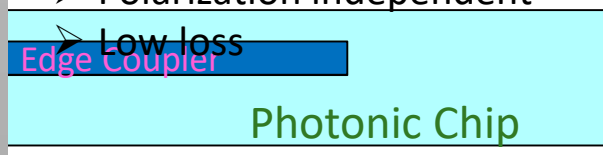
Vertical Edge Coupling: Principles of Operation



Lateral View of Probe

1. The probe is inserted into the *Dicing Lanes*
2. Total internal reflection couples light into edge couplers

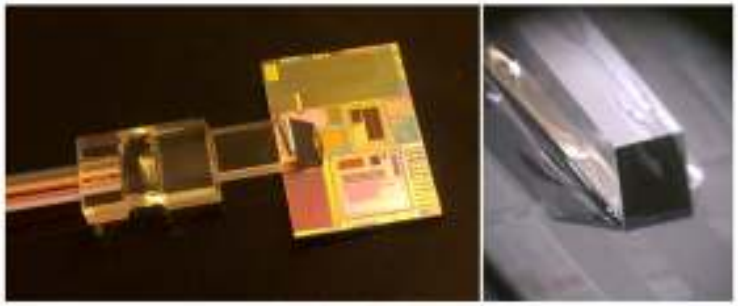
Total internal reflection
- Wavelength independent
- Polarization independent
- Low loss



Planar Lightwave Circuits (PLCs)

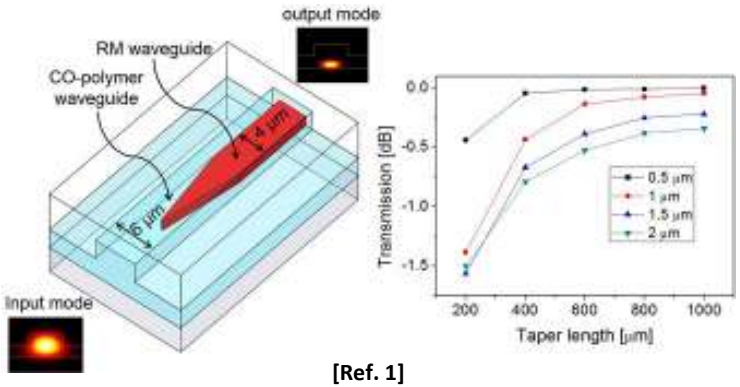
Silica substrate based integrated circuits.

- Mainly passive functionality.
  - Optical waveguide embedded in glass substrate
- Possible uses:
  - Quasi planar coupling
  - Mode matching



Top Coupling Transposer

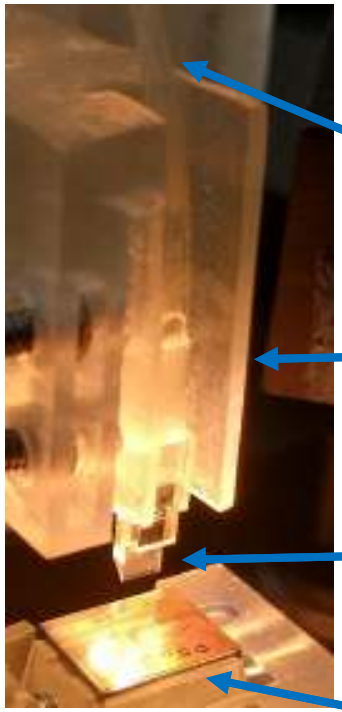
[Teem Photonics]



[Ref. 1]

Ref. 1: Huang, G., Park, T., & Oh, M. (2017). Broadband integrated optic polarization splitters by incorporating polarization mode extracting waveguide. *Scientific Reports, 7*(1). doi:10.1038/s41598-017-05324-x

Vertical Edge Coupling: Experimental Setup



Isometric View

Single Mode Fibers

Probe Holder

PLC Probe

Device Under Test (DUT)

Lateral View

Vertical Edge Coupling: Experimental Results

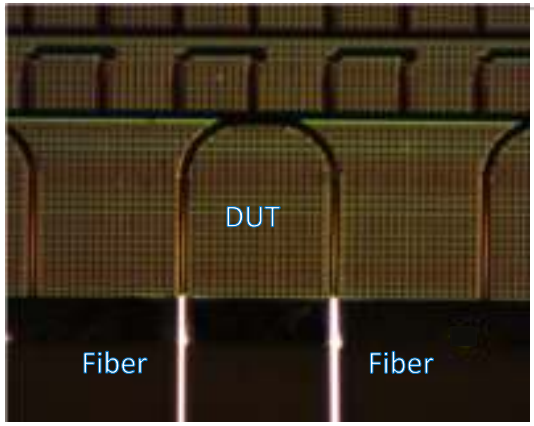


Fig 1: SMF Fiber to Chip

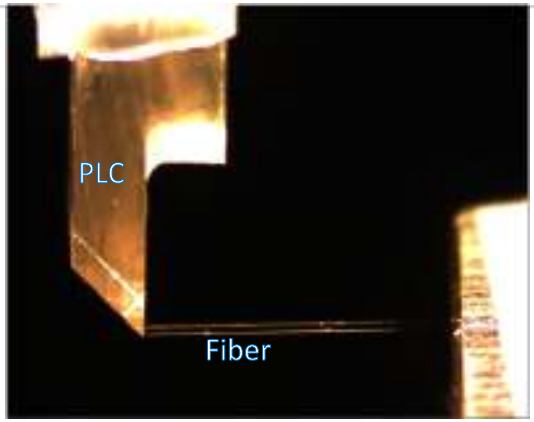


Fig 2: PLC to SMF fiber

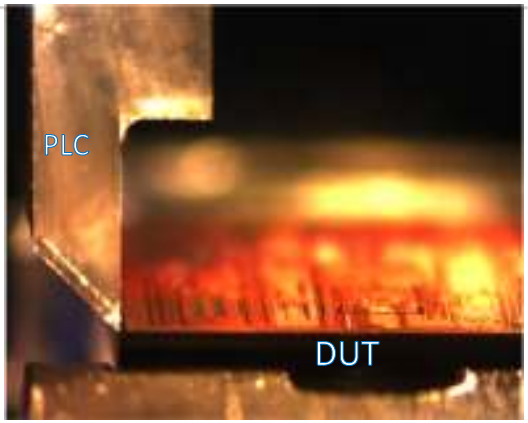


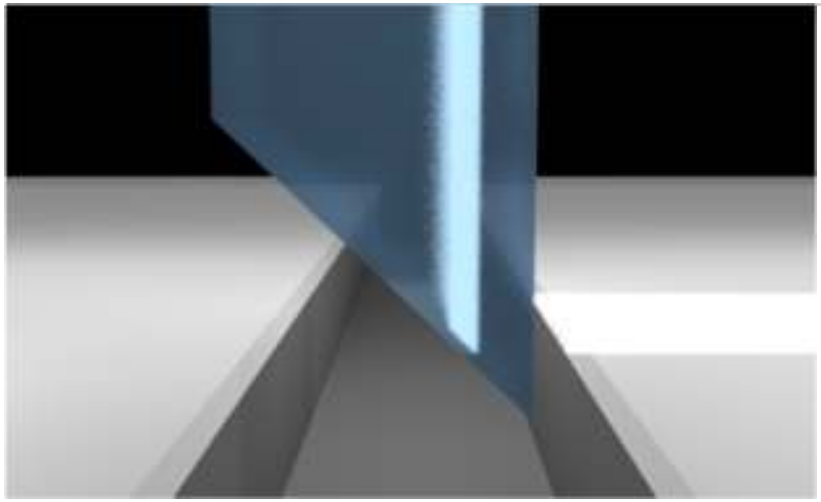
Fig 3: PLC to Chip

	SMF – AIM chip	PLC – SMF fiber	PLC – AIM chip
Injection Loss per facet [dB]	3.5	3.3	5.7
PDL per facet [dB]	9.5	0.3	11.5

Excess Loss: 2.2 dB

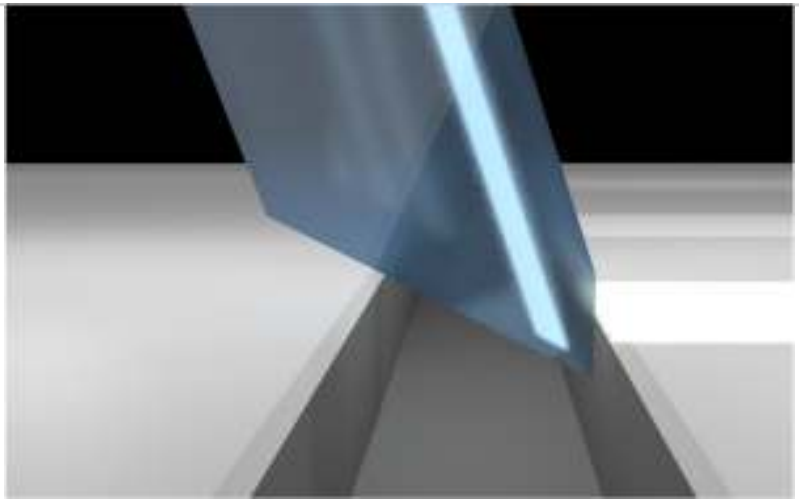
Excess PDL: 2 dB

Design Optimization



Current Design

- 45 degree reflection angle
- Waveguides buried 20 μm within substrate
- Waveguide geometry: 9 μm $\times$ 9 μm
- Mode Match: 73.4%



Next Design

- 60 degree reflection angle
- Waveguides buried 14 μm within substrate
- Waveguide geometry: 12 μm $\times$ 10.5 μm
- Mode Match: 95.9%

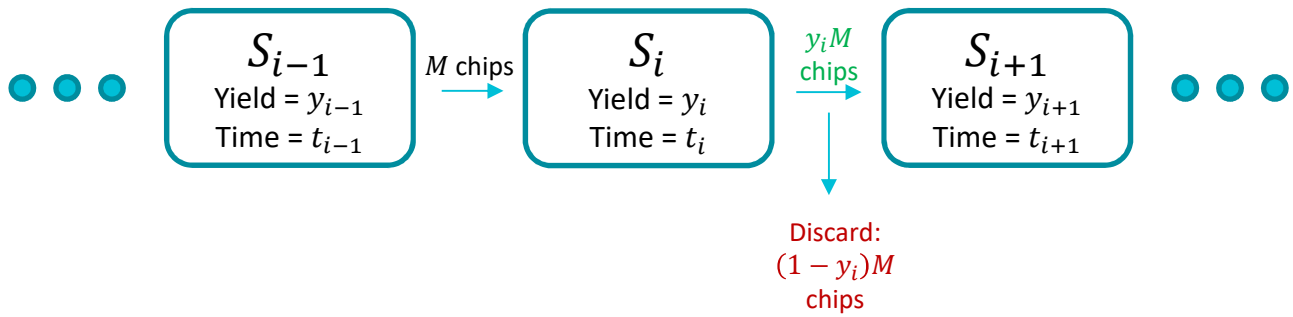
Estimated coupling improvement of 4.2 dB

Problem Formulation

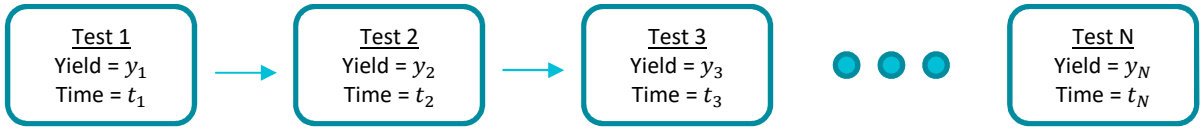
Given $S = \{S_1, S_2, S_3 \dots S_n\}$, $\quad S_i = (t_i, y_i)$

Goal: sort set S to minimize the total test time

Constraint: if the chip fails S_i, it will not be entered into S_{i+1}



Surface Level Solutions



Sort on Lowest Time

$$t_1 < t_2 < t_3 < t_n$$

Issue: if Test H has low test time, but 100% yield, it will be placed at the front, but can better minimize total test time when placed at the end.

Sort on Lowest Yield

$$y_1 < y_2 < y_3 < y_n$$

Issue: if Test H has low yield, but long test time, it will be placed at the front, but may better minimize total test time when placed at the end.

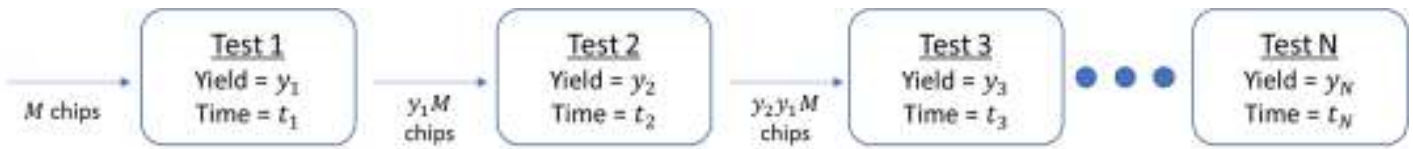
Sort on Lowest Yield-Time Product

$$t_1 y_1 < t_2 y_2 < t_3 y_3 < t_n y_n$$

Issue: Same issue as sorting by lowest time - if Test H has low test time, but 100% yield, it could be placed at the front, ced at the end.

Modeling of System May be Necessary

Total Test Time Model



$$
\begin{aligned}
&t_{total} \\
&= Mt_1 + My_1t_2 + My_1y_2t_3 + My_1y_2y_3t_4 + \cdots + My_1y_2y_3 \ldots y_{n-1}t_n \\
&= M(t_1 + y_1(t_2 + y_2(t_3 + y_3(t_4 + y_4(\ldots) \ldots)
\end{aligned}
$$

Ignore M since minimizing, and accounting for recursive nature:

$$t_{total} = T(1)$$

$$T(n) = \begin{cases} t_n \quad , & n = N \\ t_n + y_n T(n+1), & n + 1 \leq N \end{cases}$$

Mathematic Analysis

$$t_{total} = t_1 + y_1(t_2 + y_2(t_3 + y_3(t_4 + y_4(\dots)\dots)$$

Expanded:

$$t_{total_1} = t_1 + y_1 t_2 + y_1 y_2 \left(t_3 + y_3(t_4 + y_4(t_5 + y_5(\dots y_{n-1}(t_n))\right)$$

vs.

$$t_{total_2} = t_2 + y_2 t_1 + y_2 y_1 \left(t_3 + y_3(t_4 + y_4(t_5 + y_5(\dots y_{n-1}(t_n))\right)$$

When is $t_{total_1} < t_{total_2}$, but abstracted?

$$t_a + y_a\left(t_b + y_b(T_{opt})\right) < t_b + y_b\left(t_a + y_a(T_{opt})\right)$$

Solved:

$$\boxed{\frac{t_a}{1 - y_a} < \frac{t_b}{1 - y_b}}$$

Optimization Metric:

$$\frac{t_i}{1 - y_i}$$

Optimization Algorithm

Because

$$t_a + y_a\left(t_b + y_b(T_{opt})\right) < t_b + y_b\left(t_a + y_a(T_{opt})\right)$$

If

$$\frac{t_a}{1 - y_a} < \frac{t_b}{1 - y_b}$$

Then

$$Time\ of\ sequence\ S_a S_b S_{opt} < Time\ of\ sequence\ S_b S_a S_{opt}$$

Minimize Total Test Time:
Sort Tests on Optimization Metric from Lowest to Highest

Implementation Results/Considerations

Input Set | Number of chips = 100 | Output Set

```
0.12 11
0.21 10
0.36 9.5
0.45 8.2
0.52 7.1
0.6 6.6
0.72 5.1
0.84 3.2
0.90 1.3
```

```
Success #stdin #stdout 0s 4296KB
Total Time (Sort on Low Test Time): 1640.42s.
Total Time (Sort on Low Yield): 1256.72s.
Total Time (Sort on Low Yield-Time Product): 1263.24s.
Total Time (Custom Optimzation): 1400.24s.
Total Time (Recursive): 1313.56s.
Total Time (Sort on Custom Metric): 1256.17s.
```

```
0.12 11
0.21 10
0.9 1.3
0.52 7.1
0.36 9.5
0.45 8.2
0.6 6.6
0.72 5.1
0.84 3.2
```

```
0.22 11
0.11 20
0.46 5.5
0.55 9.2
0.22 7.7
0.1 6.1
0.82 3.1
0.999 1
0.992 2.3
```

```
Success #stdin #stdout 0s 4536KB
Total Time (Sort on Low Test Time): 1355.26s.
Total Time (Sort on Low Yield): 824.56s.
Total Time (Sort on Low Yield-Time Product): 744.622s.
Total Time (Custom Optimzation): 726.752s.
Total Time (Recursive): 714.792s.
Total Time (Sort on Custom Metric): 714.646s.
```

```
0.1 6.1
0.22 7.7
0.46 5.5
0.22 11
0.82 3.1
0.55 9.2
0.11 20
0.992 2.3
0.999 1
```

Conclusion

Testing Time and Power is Important

Vertical Edge Coupling = Edge Coupling + Grating Coupling

Implemented Using the Planar Lightwave Circuit

Low Cost, Efficient, Easy to Implement

Acknowledgements

This material is based on research sponsored by Air Force Research Laboratory under agreement number FA8650-15-2-5220. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon

Summary

Grating Coupling:

Advantages:
- Reduced Mode Mismatch
- Accessible on wafer scale

+

Lateral Edge Coupling:

Advantages:
- Low insertion loss
- High optical bandwidth
- Low polarization dependent loss

=

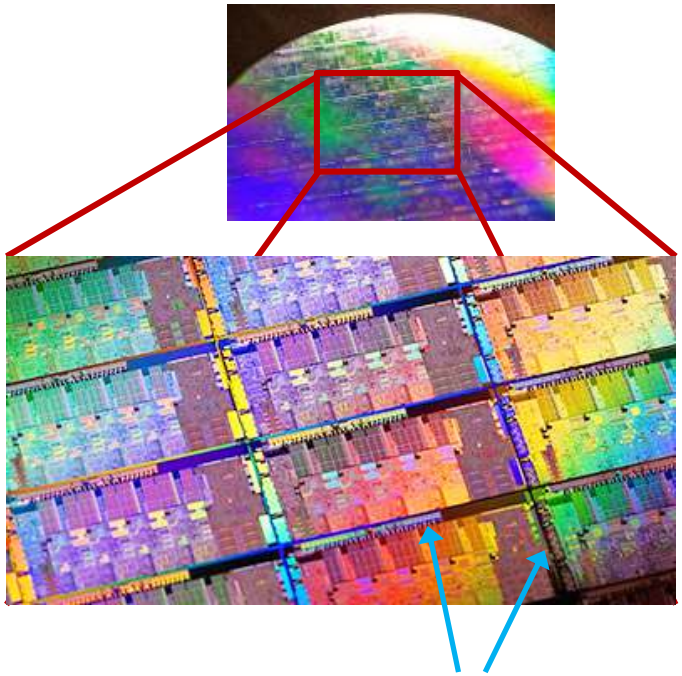
Vertical Edge Coupling:

Advantages:
- Reduced Mode Mismatch
- Accessible on wafer scale
- Low insertion loss
- High optical bandwidth
- Low polarization dependent loss

Additional Highlights

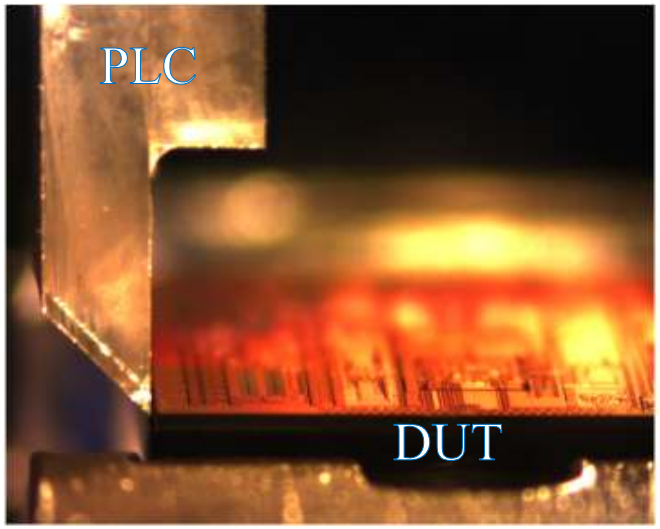
- Capable of performing high-throughput testing on wafer scale
- Requires no extra device area or change to fabrication process

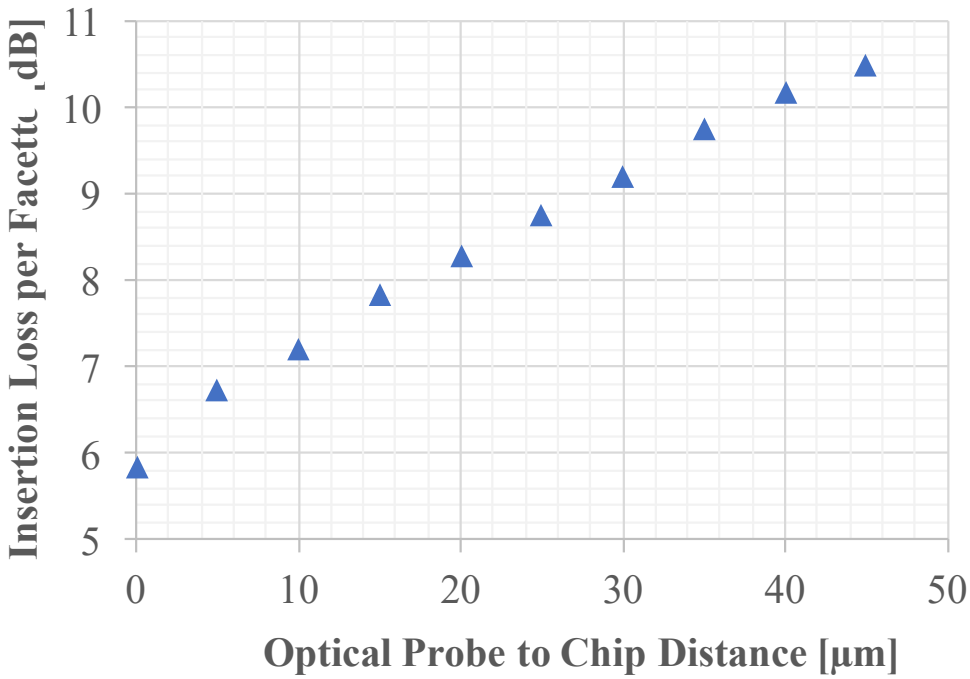
Vertical Edge Coupler: Background



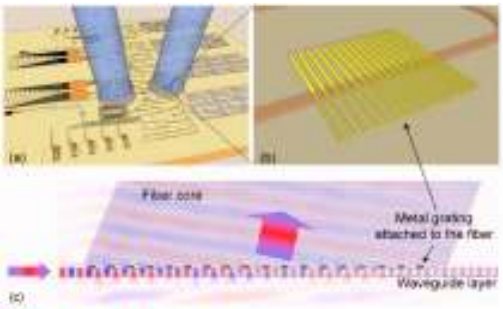
Dicing Streets: 200 μm wide, several 10th μm deep

Loss Analysis





Access Solutions

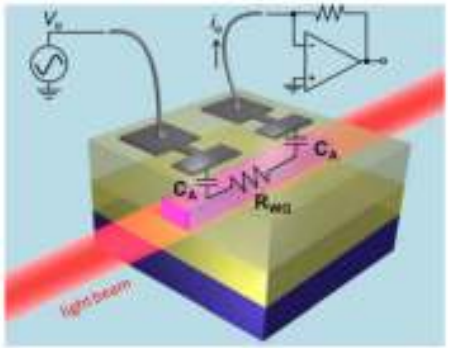


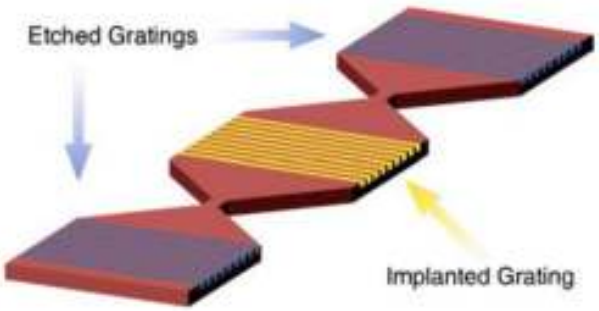
Optical fiber probe [1]:

- non-invasive
- needs direct access to waveguides

CLIPP [2]:

- non-invasive
- good sensitivity (-30 dBm)
- only DC





Erasable Couplers [3]:

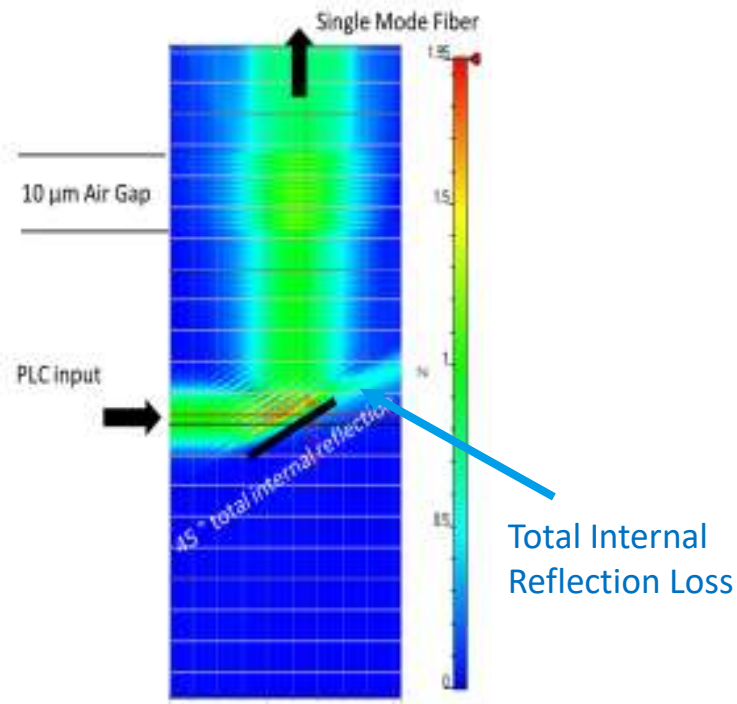
- full signal
- remaining Loss > 0.1 dB

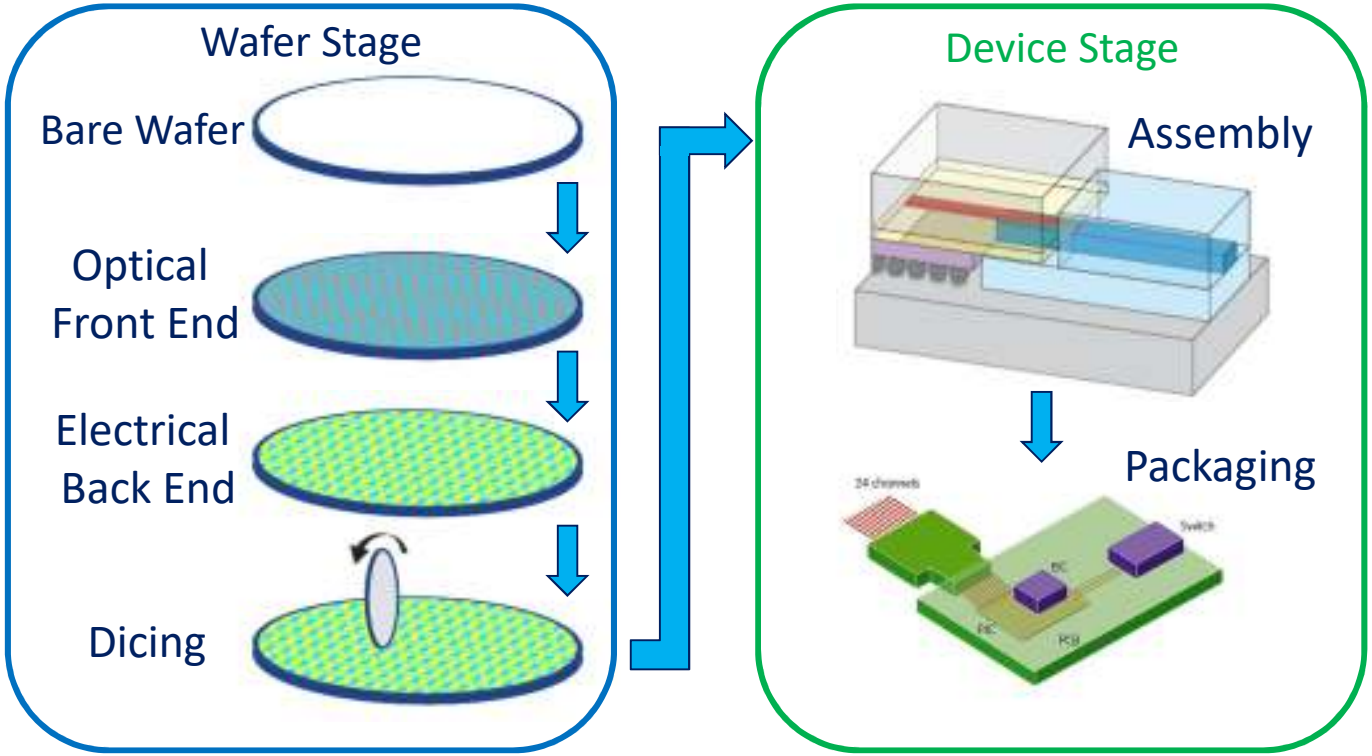
1. Scheerlinck S, et al "Flexible metal grating based optical fiber probe for photonic integrated circuits." Applied Physics Letters,92(3):031104 (2008).
2. Morichetti F, et al "Non-invasive on-chip light observation by contactless waveguide conductivity monitoring." IEEE Journal of Selected Topics in Quantum Electronics,20(4):292-301 (2014).
3. Topley R, et al "Locally erasable couplers for optical device testing in silicon on insulator." Journal of Lightwave Technology,32(12):2248-53(2014).

Vertical Edge Coupler: Coupler Loss Mechanisr

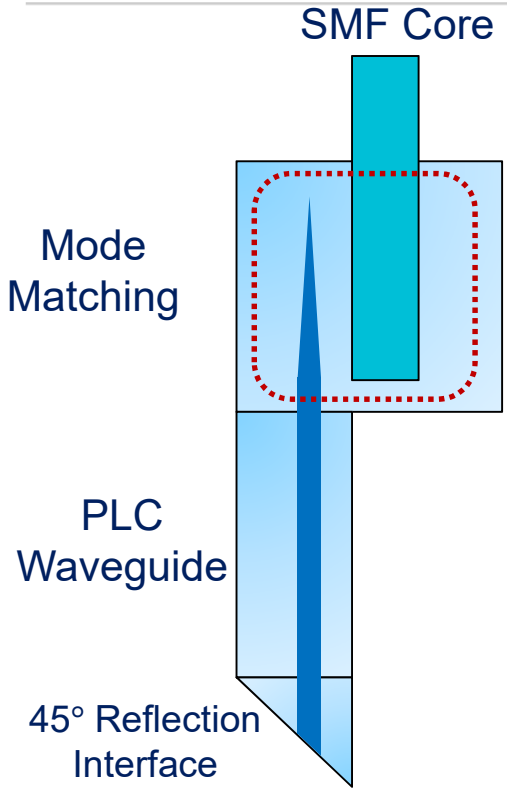
	FC/APC Connector	SMF to PLC	PLC Waveguide	Silica Air Interface
Loss [dB]	0.2	0.3	0.1	0.3

Total loss of PLC: 1.5 dB (measured)
Estimated total internal reflection loss: 0.6 dB

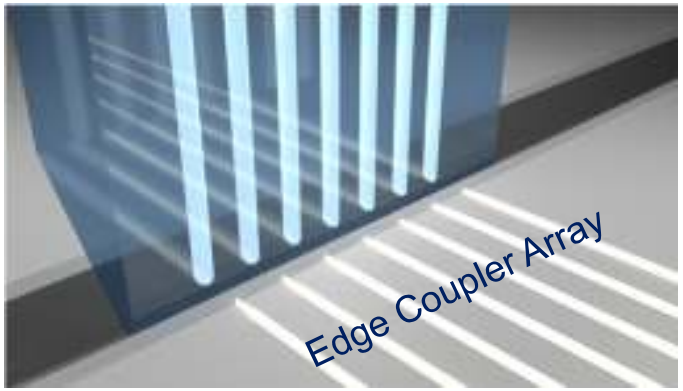



Wafer Stage
Bare Wafer
Optical
Front End
Electrical
Back End
Dicing
Device Stage
Assembly
Packaging

Vertical Edge Coupling: Principles of Operation



Lateral View of PLC

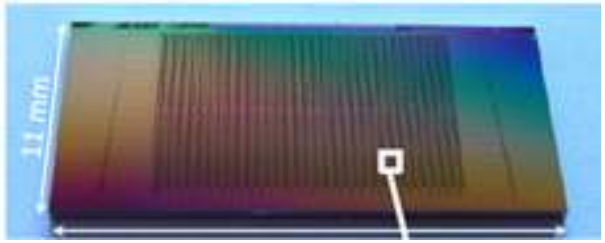


1. The PLC is inserted into the *Dicing Trenches*
2. Total internal reflection couples light into edge couplers

Total internal reflection
- Wavelength independent
- Polarization independent
- Theoretically loss-less

Testing in Silicon Photonics

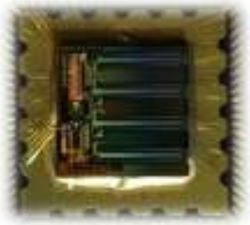
Datacom



[AIST]

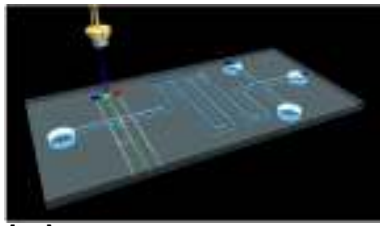
- High Port Count

Transceiver



- RF Electronics

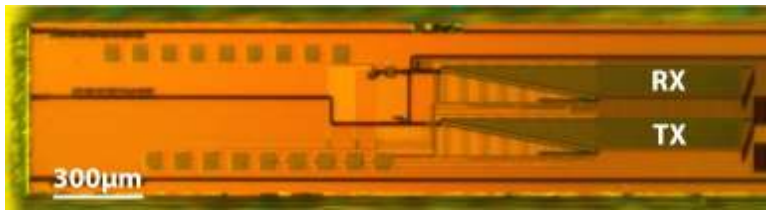
Biosensor



[KIT]

- Microfluidics Layer

LIDAR



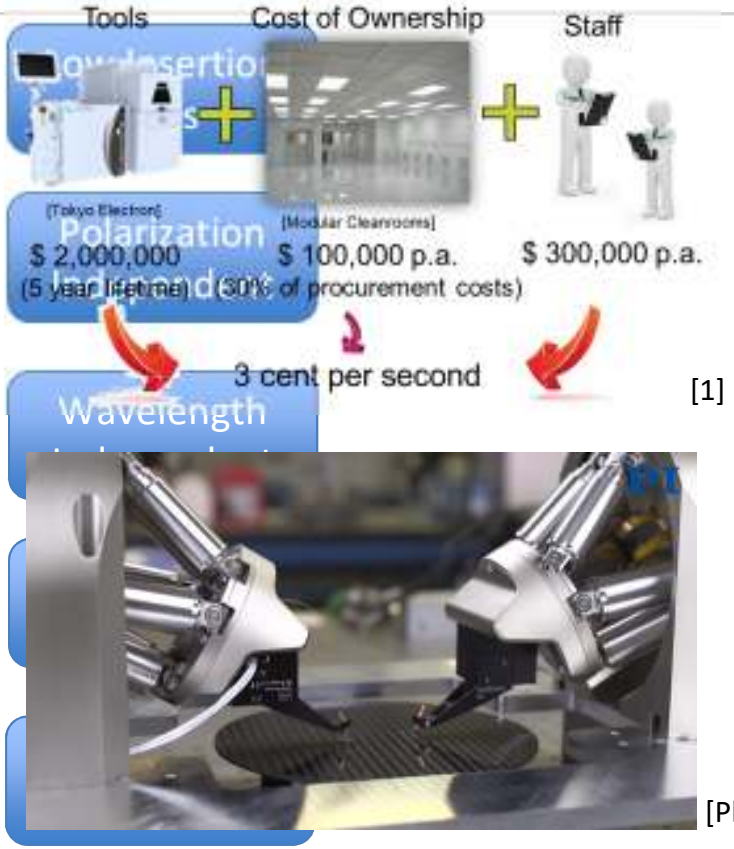
[MIT Christopher V. Poulton]

- Micro-antenna Array

Optimal Coupling Characteristics

Edge Coupling

Grating Coupling



[1]

[Physik Instrumente]

[1] Poister, R., et al. (2018). Challenges and solutions for high-volume testing of silicon photonics. Silicon Photonics XIII. doi:10.1117/12.2292235