COMPASS 2017 OVERVIEW

"Driving Test Precision Into Volume"

COMPASS 2017, FormFactor and Cascade Microtech's fifth annual users' conference, was held in Half Moon Bay, California. COMPASS 2017 delivered a highly technical content on a broad range of topics in six tracks, highlighting leading-edge applications and best practices to improve measurement accuracy and test efficiency, exemplified this year's theme, "Driving Test Precision into Volume."

Technical Tracks:

1. Advanced Testing
2. Photonics/Optoelectronics
3. RF/mmW Probing
4. Reliability/Parametric
5. Production Test
6. Power Devices

COMPASS 2017 attracted the participants from major semiconductor companies and prestigious institutions from around the globe, such as: Advantest, Analog Devices, Anritsu, Celadon, Columbia University, DMEA, Elenion, Google, HERE Technologies, imec, Infinera, Intel, International Test Solutions, Keysight Technologies, Karlsruhe Institute of Technology, Maury Microwave, ON Semiconductor, Physik Instrumente, PixelEXX, Presto Engineering, Qorvo, Qualcomm, Roos Instruments, Rudolph Technologies, SUNY Polytechnic Institute, Silicon Fidelity, Silvaco, TEL, T.I.P.S. Messtechnik, Tokyo Weld, University of California Davis, Wispry/AAC, Virginia Diodes, Xcerra and X-FAB Sarawak.

KEYNOTE SESSIONS

Day 1 Keynote

Maps for Cars by Cars

Ralf Herrtwich, Head of Automotive Business Group, HERE Technologies

Ralf Herrtwich is the Head of the Automotive Business Group at HERE Technologies. In this role, he is focused on bringing the power of HERE's Open Location Platform into vehicles as well as accelerating the deployment of location technologies to support autonomous driving. In this keynote session, he discussed issues with inaccurate and outdated maps for automated vehicles, and revealed the latest technology to keep the road maps more accurate and up-to-date by using vehicles themselves for mapping the road network in real time.

"Provide a very good overall status of mapping techniques for future auto piloting."

Day 2 Keynote

Probing and Testing Challenges in the 5G Era

Octavio Martinez, Vice President of Engineering, CDMA Technologies, Qualcomm

Octavio Martinez is in charge of product and test development for Qualcomm's RF, Power Management and Base Band Analog product lines. In his session, he gave an overview of the challenges with the evolution of 5G technology, such as higher parallelism and the emulation of the electrical characteristic of the package at the probe card / probe core, and discussed technological development to re-balance the tradeoff's in measurements accuracy (good PDN)/ KGD quality, cost of test (parallelism / ATE resources), utilization (high-current probes) and design/fabrication cycle time.

"He put the 5G topic in excellent perspective offering an excellent review and shared good insights."

TECHNICAL SESSIONS

TRACK A: ADVANCED TESTING

Magnetic Probe Cards – Hall Sensors and More

Rainer Gaggl, Ph.D. Managing Director, T.I.P.S. Messtechnik

Starting with principles of magnetic field sensors, magnetic field design and field generation, Rainer presented probe card configurations for wafer test of magnetic sensor devices with different magnetic field requirements. He showcased sample data from test floor and discussed the challenges with wafer-level testing, aspects of multi-site probing and calibration including thermal management on the probe card, and how to merge the field-generated techniques into the final test.

> *"Good review and reasonable depth of the topic and solution provided."*

Measurement Uncertainties Due to Hitherto Unspecified Offsets Between Source Measurement Units

Sebastian Koch, Development Engineer, Infineon Technologies AG

Measurement system analysis of setups involving more than one DC source reveals that although each source measurement unit (SMU) is calibrated according to specifications, measurement uncertainties can be significantly larger than expected due to unspecified potential offsets between multiple SMUs. Sebastian shared the results of a transfer characteristic measurement of a MOSFET device before and after adjustment of the potential equalization, and raised awareness of the issue which is so far neither subjected to specifications nor dealt with by regular calibration efforts. He explained that specifications, calibration possibilities or at least best-practice solutions should be provided for the common use case of employing multiple SMUs in one measurement.

Probe Card Metrology, Challenges and Solutions

Jim Powell, Applications Engineer/Technical Trainer, Rudolph Technologies

Jim reviewed the attributes of "probe card metrology solutions" to include the probe card metrology and probe card interface (or motherboard) necessary to insure the goodness of the probe test cell in manufacturing. The increasing complexity of advanced probe card solutions conspires to have probe card investment outweigh nearly any other investment in the logic probe test cell. Probe cards necessary to support the testing in high parallelism of Applications Processors and Graphics or Micro- Processors are frequently representing a meaningful fraction of the cost of the underlying test system. Ensuring the proper build/manufacture of these cards requires probe card metrology capable of substantially emulating that test system. But, more to the point, ensuring on-going performance and extending the useful life of these cards demands that users increasing invest in probe card metrology that is similarly capable.

TRACK B: PHOTONICS / OPTOELECTRONICS

Test Challenges in AIM Photonics Multi-Project Wafer Offering

Robert Polster, Post-Doctoral Researcher, Columbia University

The American Institute for Manufacturing Integrated Photonics (AIM Photonics) has been offering multi-project wafer runs, giving small businesses access to silicon photonic, and AIM Photonics will add a wafer-scale high-speed testing service for the fabricated photonic ICs (PICs) in 2018. Robert presented the design for test ideas and standards to make this testing service possible. He also showcased a wafer-scale edge-coupling technique AIM is currently developing, granting direct access to the device under test using planar lightwave circuits (PLCs), and presented first measurement results, designs and next steps.

An Approach for Wafer-Level Optical Polarization Resolved Spectral Measurements

Karl Merkel, Business Development / Application Engineer, Keysight Technologies

With the widespread move to wafer-scale production using integrated photonics technology, the throughput for testing needs to be optimized. A significant part of the time for optical testing on wafers and chips is often used for optimizing the probe coupling. During initial research and development, aligning the polarization is often manually aligned as part of the probe adjustment process while the wavelength is scanned, causing challenges with both speed and reproducibility. A powerful way to address this challenge is with fast automated measurements of the complete polarization dependence, from which the results for aligned polarization can be extracted. Karl presented the results using a swept wavelength tunable laser-based approach.

Test Station for Flexible Semi-Automatic Wafer-Level Silicon Photonics Testing

Bryan Bolt, Director of Engineering, Systems Business Unit, FormFactor

Silicon photonics technologies are a particularly attractive solution for developing low-cost optical interconnects with high performance. Bryan talked about a wafer-level silicon photonics test solution being developed with imec. The test station enables semi-automatic optical and electro-optical testing of passive and active silicon photonics components and circuits. The measured insertion loss of fiber grating couplers is repeatable to within 0.07 dB (6s), for photodetector responsivity the repeatability is around 0.02 A/W (6s). He shared wafer-level measurement data for fiber grating couplers and photodetectors that were gathered over a five-month period, showing the reproducibility of 0.8 dB for the insertion loss and 0.09 A/W for the responsivity measurement.

> *"Very interesting. Looking forward to next year's update that will feature more of the state of the art."*

TRACK C: RF/MMW PROBING

Multi-Port Millimeter-Wave (mmW) Production Test Cell

Devin Morris, RF Application Engineer, Roos Instruments

With the emergence of integrated, low-cost, high-volume mmW ICs, the need for production test capability to address this burgeoning market has become paramount to insuring market viability. Devin showcased an implemented test cell for high-density mmW production test, comprised of a Cassini 16 ATE system configured with multi-port mmW source/measure port capability with a Pyramid Probe® card and autoloading TEL probe system. His presentation demonstrated a complete production solution with on-wafer calibration standards and verified measurement performance, automated probe card calibration and thermal offset correction capability within an extensible architecture to address multiple applications from 71-86 GHz.

RF Massive Parallelism

Daniel Bock, Customer Applications and Product Solutions (CAPS) Group, FormFactor

New applications using Radio Frequency (RF) chips are driving the total number of RF lines to numbers not seen in previous generations. RF devices typically had one or two lines for transmit and a similar number for receiving. Because of the higher data rate requirements and higher operating frequencies, new applications with phased antenna arrays have pushed the number of lines up into the 20s or 30s for a single device. With the ongoing push for more parallelism in testing, Daniel thinks soon there will be a need to support probe cards with well over 100 RF lines. Daniel highlighted the new test requirements and the potential solutions to enable next-generation RF devices, as well as RF calibration considerations.

Investigation of Parasitic Modes by 3D Full-Wave Electromagnetic Simulations Including RF Probe Tips

Florian Boes, Research Associate, Karlsruhe Institute of Technology

In the millimeter-wave frequency range on-wafer measurements of passive and active circuits are prone to severe deviations between measurement and simulation. One way to achieve a better match is to perform full 3D electromagnetic field simulations (EMFS) of the devices under test (DUT). At frequencies above 200 GHz, a part of the deviation between measurement and simulation arises from the excitation of parasitic modes which are unobserved using classical EMFS techniques. Florian presented that these modes depend on the RF probe tip and thus need to be included into the EMFS simulation. By remodeling Infinity Probes tip and ISS calibration standards, a thru-reflect-line (TRL) error set based on EMFS simulations was calculated, achieving a very good agreement between measurement and simulation.

> *"Excellent use of EM software to solve a measurement issue."*

Minimizing Discontinuities in Wafer-Level Sub-THz Measurements up to 750 GHz for Device Modeling Applications

Choon Beng Sia, Customer Applications and Product Solutions (CAPS) Group, FormFactor

Achieving accurate and continuous measurement for sub-THz wafer-level device characterization is particularly important for device modelling applications. Choon highlighted the challenges affecting measurement continuity and accuracy at such high frequencies, and presented a new sub-THz measurement strategy to improve measurement continuity and quality of wafer-level measurements up to 750 GHz - with pre-calibration check for low probe contact resistance, combining power and S-parameter probe tip calibration, implementing post-calibration verification checks and ensuring consistent and accurate DC biasing of devices across all frequency bands.

TRACK D: RELIABILITY / PARAMETRIC

True Kelvin CMOS Test Structure to Achieve Accurate and Repeatable DC Wafer-Level Measurements

Choon Beng Sia, Customer Applications and Product Solutions (CAPS) Group, FormFactor

Choon presented a six-pad true Kelvin test structure for advanced CMOS devices, which allows test engineers to make accurate and repeatable wafer-level measurements required for SPICE modelling applications. This design helps to overcome parasitic resistance of the probe holder and probe which is found to be dependent on test temperatures. It also mitigates increase in probe contact resistance due to oxidation of exposed underlying copper on aluminium capped test pads as a result of repeated probing at elevated temperatures. Choon concluded that it enables accurate device measurements with minimal probe scrub, essential for 30 µm or less test pads, without the need for frequent probe tip cleaning.

Enhanced Lifetime of Copper Interconnect Lines Due to Stress Relaxation During Intermittent Current Studies

Jennifer Passage, Research Assistant, SUNY Polytechnic Institute

Jennifer showcased her study on the electromigration failure of copper interconnects using intermittent current at a previously neglected very low frequency, 10 Hz, with FormFactor's new module capable of intermittent electromigration stressing. The effects of temperature and duty cycle were studied and compared to earlier studies. Evidence of stress relaxation was revealed in significantly longer lifetimes than expected if "time on" were the only criterion for damage creation. She also discussed the consequences for extrapolation of lifetimes from accelerated to use.

Modeling and Minimizing Stray Capacitance for Parametric Probe Cards

Larry Levy, Strategic Sales, FormFactor

The stray capacitance of probe cards is starting to impact certain parametric measurements. With shrinking geometries and new test requirements, the capacitance induced by the card can become a large percent of the value we are trying to measure, thus introducing concern about the measurements accuracy. Stray capacitance in probe cards is usually measured in air. However, certain test structures in the wafer can also greatly contribute to the stray capacitance generated by the card. By localizing the values of stray capacitance produced by the main components of the probe card, Larry explained how he reengineered the card to reduce the stray capacitance significantly, while addressing the impact of potential structures in the wafer.

Overcoming Challenges of Unattended Over-Temperature Wafer-Level Measurement

Chai Kheh Aun, Process Characterization Engineer, X-FAB Sarawak SDN. BHD.

Measurements for device characterization during process development are more extensive and time consuming than production measurements. Extracting accurate device models requires a higher volume of measured data not only at ambient temperature, but also at different temperatures (-40°C to 175°C). Data collection across different temperatures can spent many hours to acquire data at each temperature. Therefore, unattended over-temperature wafer-level testing is the key to improve measurement efficiency. Chai highlighted the challenges and solutions on unattended over temperature measurement.

TRACK E: PRODUCTION TEST

The CM300, MHU300 and PDC50 in the Wafer Fab

Bart De Wachter, Test Engineer, imec

To handle high volumes of wafer probe and test, it required a probe station equipped with a wafer cassette load port/wafer handler to allow a 24/7 unattended test modus (non-stop wafer load and test). imec selected the CM300 probe station, expanded with the MHU300 wafer handling unit and a PDC50 customized probe card solution for low-resistance (<1 Ω) probe-to-wafer contacts, low-leakage levels (<pA) and tiny probe-pad scrub marks which are favored for downstream processing.

> *"Great talk - overall solution presentation how he tied it all together with the prober, probe card, use of barrel connectors and how it came together within the dark box and patch panels that eased the contact to test equipment."*

High Parallelism Probe Card on V93000 Direct Dock System to Increase Testing Throughput on Automotive ICs

Alan Liao, Customer Application and Product Solutions (CAPS) Group, FormFactor

As automotive IC fabrication process transition to sub-40 nm 12-inch wafers, customers are exploring more efficient testing solutions on the V93000 direct dock system due to increased die per wafer. Alan talked about the Matrix probe cards that FormFactor and Advantest developed for Advantest 93000 direct dock system, enabling up to 128 DUT parallel test on automotive micro-controller device at -40°C to 130°C. He highlighted extensive engineering characterization results on prober deflection and thermal behavior, high pin count probe card AOT vs. POT, and low force MEMS probe on wafer pad to achieve zero-defect IC wafer probing requirement.

A New Technology for Testing High-Speed RF Applications within Texas Instruments

Patrick Rhodes, Product Engineer, FormFactor

High-speed testing has been a specialized area that not every probe card supplier is able to play in. There is much to be studied and understood in both design of board and also repeatability of measurements due to sensitivity of application for high volume, large site count probing. Texas Instruments compared the performance of FormFactor's Katana RFx technology to the membrane-based Pyramid Probe cards. Patrick explained how Texas Instruments compared these two probe card technologies on the same device to look to provide another option for RF testing using the Katana RFx pin.

TRACK F: POWER DEVICES

Role of Wide Bandgap Semiconductors in Next-Generation Power Converters

Srabanti Chowdhury, Professor, Department of Electrical and Computer Engineering, University of California Davis

Professor Chowdhury discussed the recent progress in Gallium Nitride (GaN)-based power electronic devices. Reducing conversion losses is not only critical for minimizing consumption of limited resources, it simultaneously enables new compact architectures, the basis for a new industry offering increased power conversion performance at reduced system cost. GaN-based Photovoltaic (PV) inverters have achieved efficiency above 98% at a pulse-width modulation frequency of 50 kHz (vs. 96% with Si at 15 kHz), reducing loss by 50%, thereby shrinking the PV inverter size by 40%. While lateral GaN devices are more matured in technology and have entered the medium power conversion market (up to 10 kW), vertical GaN devices are evolving to address high power conversion (10 kW-10 MW). She explained that the novelty of the device design can be extended beyond GaN to other wider bandgap materials like Gallium Oxide, Aluminum Nitride and Diamond for more futuristic power and other novel fields like photovoltaic and GHz-THz frequency applications.

> *"Deep technical insight normally not seen from probe card maker's perspective."*

Forget the Paschen and Embrace Turbulence!

Adam Schultz, Electrical Engineer, Celadon Systems

Paschen's Law has historically been used by engineers as the reference curve for voltage breakdown as a function of gas pressure and gap distance. Celadon, jointly with Keithley Instruments, revealed unexpected and compelling results regarding Paschen's Law, as well as a surprising correlation between high-voltage "soft fails" and Time Dependent Dielectric Breakdown (TDDB) reliability testing techniques. Direct Jet™ was presented as part of the overall test solution to suppress surface arcing to prevent damage to the device.

Latest Advancements in High-Power Device Test Technology

Gavin Fisher, Senior Application Engineer, Customer Application and Product Solutions (CAPS) Group, FormFactor

Power device test has been always a challenging task, either at package or wafer level, requiring tools that can endure extremely high-current and high-voltage conditions. As the demands for devices with higher energy efficiency rapidly grow, the device manufacturers are forced to test devices at even higher current and voltage conditions with shorter time. Gavin featured the latest high-power test solution that helped Cambridge University achieve the measurement never possible before.

INTERACTIVE WORKSHOP

For the first time, COMPASS offered educational workshop sessions. The workshop was offered as modules, to keep the class size small and encourage open discussions. Through the lively conversations, our subject experts shared their experiences and knowledge and practical tips with the participants.

1. **Millimeter-Wave Solution for On-wafer Measurements** *(Giancarlo Dechirico, Keysight Technologies)*

   Giancarlo reviewed the key aspects of a mmW VNA, and explained the hardware architecture of the solution focusing on the key performance parameters that enable on-wafer measurements, as well as how to optimize the measurement of on-wafer devices and components.

2. **Prober Implementation for mmW On-wafer Measurements at 120 GHz** *(Gavin Fisher, FormFactor)*

   Gavin showcased an example of how to automate the process of moving mmW probes on multi-device layout using programmable positioners, and how the new chuck enclosure can reduce insertion loss and improve raw directivity and stability by minimizing cable length. He showed system stability as a function of time, calibration repeatability, and made a cross comparison of device measurements from one system to another.

3. **RF Multi-Site Calibration** *(Daniel Bock, FormFactor)*

   Daniel reviewed how to get the most out of the use of Keysight VNAs in order to get an excellent RF calibration in multi-port probing designs.

4. **How to Optimize Probe Card Touchdown** *(Alan Liao, FormFactor)*

   The optimized touch down has a direct impact on the overall cost of test and yield. In this session, Alan reviewed factors that could affect the touchdown and discussed how your probe card touchdown can be improved.

5. **Probe Card Selection Guide** *(Alan Liao, FormFactor)*

   There are various types of applications in the market today that require different set of probe card capabilities for their wafer test. Each probe card technology has different set of capabilities and cater to specific design requirements such as speed, pitch, pad/bump type and parallelism. Alan reviewed the selection of probe technology based on the application space and cost of ownership.

6. **Adjustable Multi-Site Probing Solution for WLR Testing** *(Eric Wilcox, FormFactor)*

   Traditional 4.5" and full wafer multi-site probe cards for WLR testing have fixed test sites with no adjustability, thus the probe card is designed specifically for one wafer layout, and additional probe cards are required for each wafer with a different layout or die size. Eric reviewed a multi-site probing solution that addresses this challenge by achieving independent adjustability for each of the test sites.

7. **Cleaning Solutions for FormFactor Probe Cards** *(Doug Ondricek, FormFactor)*

   Doug reviewed the options for online and offline cleaning of various FormFactor probe technologies, and discussed why cleaning is needed and the recommended cleaning solutions for our various probes. Also, he examined a trade-off between maintaining stable CRES and maximizing probe lifetime.

8. **Ultra-High Parallel Test Enabled through Tester Resource Enhancement** *(Michael Huebner, FormFactor)*

   Most probe cards for memory device test (DRAM of Flash) take advantage of Tester Resource Enhancement (TRE) or Advanced Tester Resource Enhancement (ATRE). TRE is generally a split of control signals where ATRE technology generally uses multiplexing circuits to use DC and power resources on multiple DUTs. Michael reviewed the basic aspects of TRE and ATRE, a detailed overview of the implementation, control and capabilities of circuits on ultra-high parallel memory probe cards.

SPONSORS EXPO

COMPASS sponsors showcased their products and services during the Sponsors Expo.

NETWORKING EVENTS

Learning opportunities through networking are one of the most important aspect that the COMPASS attendees value. COMPASS 2017 offered many networking opportunities throughout the conference, giving the participants a chance to connect with their industry peers and discuss the future of the test and measurement technology with industry leaders.

Birds of a Feather Roundtable Lunch
The attendees enjoyed lively discussions and sharing their insights on the applications of their interest, such as:

- Production Test
- RF/mmW Probing
- Calibration
- High-power Device Test
- Reliability/Parametric Test
- Photonics/Optoelectronics

Offsite Event and Group Dinner
Half Moon Bay offered the participants a guided nature walk around the Half Moon Bay and a kayak tour in the calm waters of the harbor, followed by a casual Italian dinner.

Happy Hour
COMPASS 2017 closed with a happy hour at the Half Moon Bay Brewing, where guests enjoyed local microbrews under the sun.

ACKNOWLEDGEMENT

We would like to thank COMPASS 2017 committee members and sponsors:

Steering Committee

- Noam Ophir, Elenion Technologies
- Jens Klattenhoff, FormFactor
- Amy Leong, FormFactor
- Junko Nakaya, FormFactor
- Robert Selley, FormFactor
- Laurie Winton, FormFactor

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- Mary Katchur, Intel
- Joel Orona, ON Semiconductor
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- Gavin Fisher, FormFactor
- Alan Liao, FormFactor
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