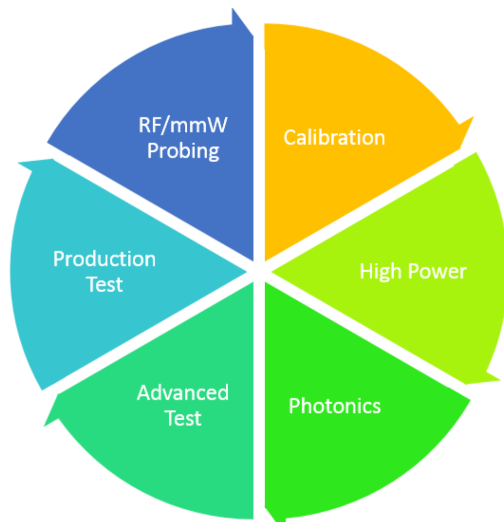
COMPASS 2016 OVERVIEW

Cascade Microtech's fourth users' conference, COMPASS 2016, successfully closed with record attendance. For the first time, the conference was held in Portland, Oregon, allowing attendees to visit Cascade Microtech campus in Beaverton for interactive equipment demonstrations.

With six application-focused tracks, including the new optoelectronics/photonics track, COMPASS offered a broad range of topics that highly resonated with the attendees from a variety of major semiconductor companies and prestigious institutions such as: Advantest, Analog Devices, Apple, Celadon, Coriant, Dominion MicroProbes, Graz University, IHP, Infineon, Intel, inTEST, Keysight Technologies, Karlsruhe Institute of Technology, Maury Microwave, Maxim, NXP Semiconductors, ON Semiconductor, Portland State University, Physik Instrumente, Qorvo, R&D Altanova, Rockley Photonics, Roos Instruments, Skyworks, Texas Instruments, T.I.P.S. Messtechnik, Tektronix, Teraview, Texas Instruments, Virginia Diodes, W.L Gore, Xcerra and X-FAB Sarawak.



COMPASS 2016 covered a diverse range of applications.

COMPASS 2016 delivered a substantive level of technical content on a broad range of topics, highlighting advanced device measurements and technology development. The presentations of cutting-edge technologies and unique applications to support the future of the test and measurement industry, as well as best practices to improve measurement accuracy and test efficiency, exemplified this year's theme, "Conquering Tomorrow's Test Challenges".

- "*Very well run. Congratulations!*" *(Intel)*
- "*Thoroughly enjoyed the conference and the events planned around it.*" *(Texas Instruments)*
- "*Thank you for another well done conference.*" *(Analog Devices)*

OPENING KEYNOTE

Capex to Opex Economics within the Internet of Things

Michael Murray, General Manager, Industrial Sensing Division, Analog Devices

Analog Device's keynote session was very well received and the audience showed a great interest in learning about Analog Device's Intelligent Factory experiment and an overview of the Global Connect Initiative 2020 program by the White House. Michael explored both the technological and economical boundaries and potential within the greater IoT market with a distinct focus on intelligent factories and the system within them. He shared his learnings, both successes and failures, from this experiment, including the economic balance of the value of instrumenting certain equipment or instruments inside an operating factory and the return on the investment.

- "*Very thought provoking.*" (Maxim)
- "*Intelligent Factory experiment was eye-opening.*" (Texas Instrument)

FEATURED PRESENTATION

Test Challenges for Integrated Optics

Noam Ophir, Design Verification Testing Team Lead, Coriant Advanced Technology

Integrated optics, and in particular silicon photonics, poses unique test challenges. As the industry moves toward building large-scale integrated photonic devices, a very rapid evolution of the relevant test platforms is going to be required. Noam discussed challenges associated with driving down test costs and improving yields, along with an overview of the state of photonic and optoelectronic testing today.

TECHNICAL SESSIONS

TRACK A: CALIBRATION

Near and Far Field E and H in Sub-mmWave On-wafer Probes
Rick Campbell, Professor, Portland State University

Thinking in wavelengths instead of microns, Rick reviewed the basic E and H theory and the radiansphere, and presented a few near-field measurements of E and H components around a scale model wafer probe tip. He then discussed how to use what we have learned to improve accuracy and reliability of on-wafer sub-mmWave calibration and measurements.

- "*Would like an extended talk on this or more detailed paper.*" (Maxim)

A Method for On-wafer Calibration of Power and Impedance
Suren Singh, Application/Product Marketing Engineer, Keysight Technologies

Suren showcased a novel method of power calibration at the probe tip for an on-wafer active device measurement by reviewing the system architecture and the method for power calibration using Keysight PNA / PNA-X with Cascade Microtech's WinCal XE™ software. He presented different methods used in the calibration and their limitations, stepping through the process steps and presenting supporting measurement data.

Comparison of Calibration Processes with a Precise On-wafer Measurement System in NMIJ
Ryo Sakamaki, Research Scientist, National Institute of Advanced Industrial Science and Technology (AIST)

AIST investigated transmission and reflection characteristics of calibration standards providing to difference of measurement results obtained by a precise on-wafer measurement system. Ryo presented that different verification results have relevance to operational variation in calibration process. He focused on effects of highly reflected calibration standards, i.e. open and short circuits, to measurement results of KVS (Keysight Verification Substrate), and reviewed the comparison results of calibration methods in evaluation of verifications devices.

TRACK B: HIGH-POWER APPLICATION

High Voltage, High Current - and Some Like it Hot Too…
Rainer Gaggl, Ph.D., Managing Director, T.I.P.S. Messtechnik

Recent developments in power semiconductor technology and numerous activities in the field of Si, SiC and GaN based devices have driven the need for power tests at high temperature. Rainer highlighted some aspects of gas discharge physics with special attention to effects at elevated temperature, and showcased probe card configurations that address these requirements.

Unique Approach to Characterizing Power Devices at 3 kV over Temperature
Bryan Root, President and CEO, Celadon Systems

The automotive industry is driving the need for high-power semiconductor devices. This push has resulted in numerous high- current and high-voltage applications in the industry. To keep pace with these applications the ability to test up to 3kV and over wide temperature range is critical to properly test and characterize these devices. Bryan discussed the successful implementation of a versatile system using Celadon 45e and VC20 probe card coupled with the Keithley 2657A Sourcemeter SMU instrument.

Advancing the Frontiers in Automatized On-wafer Testing of Power Semiconductors
Peter Andrews, Director of Market Development, Cascade Microtech

The rapid development of power semiconductors, such as IGBTs and power MOSFETs, has been challenging the limits of testing and probing device properties, as they reach ever faster switching speeds and higher current and electric field densities. Furthermore the utilization of novel materials such as SiC and GaN are enabling devices that can operate at temperatures well beyond the critical 175°C of Si and switching frequencies in the tens MHz. Peter presented the joint efforts of Fairchild Semiconductor and Cascade Microtech on developing on-wafer methods for three future challenges: automatized high-temperature electric testing, dynamic on-wafer testing and high power on-wafer testing.

TRACK C: RF/mmW PROBING

High-speed and Wideband On-wafer Load Pull for Model Extraction, Validation and Design
Gary Simpson, Chief Technical Officer, Maury Microwave

Load pull is an essential tool in the large-signal characterization of high-frequency devices, however, common passive and active load pull techniques are highly demanding in measurement time, especially when it is desired to monitor and control multiple parameters simultaneously. Gary introduced a mixed-signal active load pull approach that reduces hours of measurements to just minutes in single-tone CW and pulsed-CW operation, and enables instantaneous wideband impedance control up to 240 MHz for modulated load pull operation.

Landing Pads for Measuring PCBs up to mm-Wave Frequencies using a Probe Station
Dr. Michael Gadringer, University Assistant, Institute of Microwave and Photonic Engineering, Graz University of Technology

In this presentation, Michael discussed the challenges imposed by measuring PCBs using commercially available mmW probes, such as Cascade Microtech's ACP probes. To overcome the challenges introduced by the RF laminates and the corresponding manufacturing processes, a new landing pad design for measurements from DC up to 100 GHz was investigated. He showcased the different versions of the landing pad to verify the results from the simulations, and reviewed the impact of the manufacturing tolerances on the performance of the landing pad.

Optimizing On-wafer THz and Differential Measurement Accuracy with High Directivity
Jeffrey Hesler, Chief Technical Officer, Virginia Diodes

As the frequency of test increases, losses in waveguide sections and on-wafer probes can become a significant issue. Since a reduction of system directivity affects overall on-wafer system performance, calibration repeatability and system drift, having the probe tip closer to module output flange but yet being able to contact the device under test is thus a desirable attribute. Jeffrey discussed how the optimized high-frequency extenders can reduce this distance, and improves the dynamic range thus measurement results at 500 GHz up to 1.1 THz frequencies.

Investigation of Line Length Effects in Multiline TRL Calibrations at 1.1 THz
Matt Bauwens, Senior Engineer, Dominion MicroProbes

Recently advances in the development of THz device technologies have created a need for on-wafer probes operating at THz frequencies. At such high operating frequencies, spurious effects such as radiation have an increased effect on calibration and measurement quality. Matt highlighted the effect of line lengths in multi-line TRL calibrations at 1.1 THz, shared measurement results by comparing electromagnetic simulation models, and gave recommendations on line lengths.

TRACK D: PRODUCTION TEST

Production-level On-wafer Probe of Multi-channel 77 GHz Radar Transceiver Chipset
Jeffrey Finder, ADAS Product and Test Engineering Manager, NXP Semiconductor

Radar-based active safety systems are in the automotive market today, enabling key applications such as emergency braking, adaptive cruise control, blind-spot monitoring, and cross-traffic alert. Jeffrey introduced NXP's MR2001, a high-performance 77 GHz radar transceiver chipset that is scalable for multi-channel operation, enabling a single radar platform with electronic beam steering and wide field-of-view for long, mid-, and short-range radar applications. He then described the challenges and results of production-level on-wafer probe of 77 GHz devices using the Pyramid-MW probe card, as well as the impact of membrane core properties, membrane wear, contact resistance and probe pad surface on measuring critical RF parameters at 76 - 77 GHz.

Verification of High-Bandwidth-Memory (HBM) through Direct Probing on MicroBumps
Michael Huebner, Sr. Director of Product Marketing, FormFactor

High-Bandwidth-Memory (HBM) is a new type of memory that promises low power consumption, and ultra-wide communication lanes to improve system-level performance. HBM also leverage innovative 2.5D and 3D stacking technologies which brings in many new possibilities and challenges from test perspectives. Michael reviewed the electrical challenges and simulation results associated with direct on MicroBump probing of wide data busses at up to 1 GHz, as well as how MicroBumps respond to the probe card under various probing conditions such as current, test temperature and test durations.

Production Millimeter-wave Test Cell for Automotive Radar SoCs
Devin Morris, RF Applications Engineer, Roos Instruments

To facilitate the growth of millimeter-wave automotive radar as a standard safety feature, ICs and System-on-Chip (SoC) transceiver architectures are being developed in standard CMOS processes to deliver integrated, low-cost, high-volume 77 GHz radar. Devin showcased a production millimeter-wave test cell to address the rigorous testing demands of SoC automotive radar chipsets at wafer level, comprised of a Cassini 16 ATE system, CM300 probe station and Pyramid Probe® card.

- "*Strong presentation. Good knowledge of the test cell and its architecture.*" (Texas Instruments)

Achieving Higher Speeds for CMOS Image Sensor Testing
Larry Levy, Senior Director, Strategic Sales, FormFactor

CMOS image sensor market continues to grow at ~10% CAGR, and a part of this market is driven by the need for higher and higher speed. Larry showcased how FormFactor and Hitachi Chemical, using new PCB materials and design rules, were able to achieve loss characteristics comparable to traditional high-speed CIS probe card performance without a lens module, and exhibited an Eye pattern simulation that used actual S-parameter data, indicating they were able to meet enough signal quality for 3 Gbps. He also discussed what structural changes may be required for the next future target of 5 Gbps.

TRACK E: ADVANCED TESTING CHALLENGES

Advanced Measurement and Processing Capability within WinCal XE
Gavin Fisher, Senior Applications Engineer, Center of Expertise, Cascade Microtech

Gavin reviewed how some of the advanced tools in WinCal XE that may help users, such as full-wafer RF test including DC bias and sending key metric data back to the WaferMap using the built-in sequencing functionality with its simple programming language. He demonstrated how WinCal XE creates detailed post-processing functions such as modifying the calibration method of an entire set of data after measurement to view ramifications of error term variation.

Applications and Measurement Considerations on Low-frequency Noise Analysis
Raj Sodhi, Applications Developer, Keysight Technologies

To minimize the effects of electrical noise inherent in every circuit, it is necessary to measure and quantify the noise of the constituent parts, and then connect the constituent noise contributions to overall circuit performance. Raj reviewed the basics of noise spectral density, noise measurement applications, practical considerations in noise measurements, and how the Advanced Low-Frequency Noise Analyzer (A-LFNA) in combination with WaferPro Express measurement software addresses these challenges. He also shared the best practices that may help to reduce the typical problems encountered when doing wafer-level measurements of low-frequency noise.

- "*Very educational. Enjoyed it.*" (Roos Instruments)

Challenges in Package-Level Reliability (PLR) Testing for EM, SM and HCI
Ng Hong Seng, Group Manager, Reliability Testing, X-FAB Semiconductor Foundries

In the level1 process reliability testing, wafer-level reliability (WLR) test is typically a preferred method, however, package-level (PLR) test is still unavoidable in process qualification, because PLR provides more accurate lifetime extrapolation through higher sampling rate and longer stress time. In this session, the challenges encountered for PLR EM, SM and HCI and the solutions to address these challenges were discussed. Both WLR and PLR methods on different via and metal line structures on AlCu scheme were studied, as well as the correlation between WLR and PLR for MOSFET devices with standard LV NMOS and MV LDMOS device.

TRACK F: OPTOELECTRONICS/PHOTONICS

An Approach to Wafer-level Characterization of a Planar Opto-electronic BiCMOS Technology
Marcel Kroh, Scientist, Technology/Si Photonics, IHP

To date optoelectronic components are manufactured based on a broad choice of materials. Among those materials silicon has gained particular interest due to the potential of monolithic integration of optics and high-speed electronics. In this session, a planar optoelectronic BiCMOS integration technology based on Silicon-on-Insulator was presented, including a brief description of its possibilities, and examples for the on-wafer investigation of optoelectronic devices, reflecting the broad application space of this technology.

Out of the Lab and into the Fab: Optical Probing as an Enabler for Silicon Photonics' Next Chapter
Scott Jordan, Sr. Director, NanoAutomation Technologies, Physik Instrumente (PI)

Silicon photonics technologies are approaching critical implementation phases for volume production. This poses significant fresh challenges for testing in the engineering and developmental stage and in planning for repetitive manu-facturing. A key impediment has been the need for nanoscale-accurate physical alignment of optical fibers and devices in test and packaging processes. Scott reviewed its profound effect

on optical throughput, and optical probes. Alignment must be active and for many tests must be capable of tracking device drift due to thermal and other disturbances. Prior approaches to this challenge have not been suitable for the multiple inputs and outputs commonly encountered in today's SiP devices, nor was their speed sufficient for these applications. Scott highlighted a novel, multichannel-capable active alignment solution has been integrated into wafer probers optimized for developmental and engineering test and measurement.

Silicon Photonics Market Trends and Cascade Microtech's Roadmap
Dan Rishavy, Director of Market Development, Cascade Microtech

The transition from photonic devices manufactured in exotic semiconductor processes into standard silicon technologies is underway. Dan explained how measuring test structures and photonic components at the wafer level is critical, and why an integrated solution that includes high accuracy automated fiber positioning coupled with a high rigidity and vibration-isolating probe station is important to ensure the fastest time to measurement. He also reviewed Cascade Microtech's current and future endeavors on developing a standardized test methodology to lower the cost of wafer-level photonic measurements.

INTERACTIVE EQUIPMENT DEMO

For the first time in COMPASS history, participants were invited to Cascade Microtech facility in Beaverton for live equipment demonstrations, featuring the following applications:

- Two-port measurement and calibration at 110 GHz
- Automated multi-site wafer-level reliability test
- Silicon photonics probing
- Automating small-pad probing down to 30 µm with accurate PTPA
- Parametric probe card for automotive radar and SoCs
- 1/f device noise characterization

The participants enjoyed watching the live equipment demonstrations by subject experts who prompted lively discussions.

SPONSORS EXPO

This year's COMPASS sponsors added value to the conference through showcase of their products and capabilities during COMPASS Sponsor Expo.

NETWORKING EVENT

Learning opportunities available from networking with fellow attendees and Cascade Microtech's technical experts are the two values most highly rated by participants. COMPASS 2016 offered many networking opportunities during the event, beginning with the welcome reception on the first day to the happy hour after closing the event, giving the participants a chance to get to know their industry peers and discuss the future of the semiconductor industry with top global industry leaders. Some of the highlights include:

Birds of a Feather Roundtable Lunch
The attendees were able to have lunch with other attendees and Cascade Microtech experts who share common interests in particular topics, such as:

- Production Test
- RF/mmW Probing
- Calibration
- High-power Application
- Reliability Test
- Photonics/Optoelectronics
- Advanced Testing Challenges

During the lunch, the attendees were able to have enthusiastic discussions and share their experiences and ideas.

Haunted PDX Brewery Tour and Group Dinner
The participants enjoyed PDX haunted brewery tour, although they got rained on at the end of the tour (but that's a part of Portland experience!).

After the tour, they enjoyed dinner at Fogo de Chao, a famous Brazilian steak house in downtown Portland.

Happy Hour
After coming back from the live equipment demo sessions at the Cascade Microtech campus in Beaverton, COMPASS 2016 closed with a Happy Hour Reception, where guests stayed well into the evening to enjoy talking shop and connecting.

ACKNOWLEDGEMENT

We would like to thank everyone who participated this year:

Steering Committee

- Mehrdad Baghaie, ON Semiconductor
- Amy Leong, FormFactor
- Junko Nakaya, Cascade Microtech
- Laurie Winton, Cascade Microtech

Technical Committee

- Jason Alikpala (chair), Cascade Microtech
- Sebastian Giessmann (chair), Cascade Microtech
- Jory Twtichell, NXP Semiconductor
- Micki Marion, Broadcom
- David Newton, Cascade Microtech
- Eric Wilcox, Cascade Microtech
- Gavin Fisher, Cascade Microtech
- Koby Duckworth, Cascade Microtech
- Ruben Zowada, Cascade Microtech

Sponsors

COMPASS 2017

Watch for updates at compass.cascademicrotech.com, and if you would like to present at or participate in the committee at COMPASS 2017, please contact us at compass@cmicro.com.

We hope to see you at COMPASS 2017!