COMPASS 2014 Executive Summary

Overview

Held at the end of the European Microwave Week (EUMW) in Rome, Italy, Cascade Microtech’s second users’ conference delivered a substantive level of technical content on a broad variety of probing topics. COMPASS 2014 attracted users from across the globe to share test challenges and solutions, and network with their peers as well as Cascade Microtech technical experts and executive management.

The event comprised the following elements:

- Case-study presentations by a diverse set of customers, which highlighted advanced device measurements and technology development supported by Cascade Microtech.
- Cascade Microtech’s technical presentations co-authored by customers, showcasing best practices and cutting-edge technologies to support the future of the test and measurement industry.
- Networking opportunities and information sharing during roundtable lunch and evening receptions, as well as during sessions.

COMPASS 2014 presentations covered a broad range of applications:

- **Advanced Techniques**
  - On-wafer MMICs testing
  - Multi-site WLR test
  - Noise measurements
  - Electromigration testing of BEOL CMOS

- **Fine-Pitch Probing**
  - Fine-pitch micro-bump probing
  - Over-temperature small-pad probing
  - Improving signal integrity

- **High-Power Device Characterization**
  - On-wafer GaN characterization
  - Measurement at high temperature
  - Capacitance characterization
  - Instrumentation and prober configuration for on-wafer power device characterization

- **Sub-THz Probing**
  - On-wafer sub-THz antenna probes
  - 750 GHz VNA extenders
  - RF test cell repeatability and accuracy
COMPASS 2014 attracted test engineers and device designers from leading semiconductor companies

The overall attendee mix represented a broad cross-section of industries leading to dynamic discussions among the attendees throughout the event.


Opening Keynote

The New “IC” – Innovation and Collaboration – and its Impact on Test

John Y Chen, NVIDIA

Dr. Chen has been in the semiconductor industry for over 36 years and has served as the Vice President of Technology and Foundry Operations at NVIDIA Corporation, the world leader in visual computing technologies, for over ten years. Prior to joining NVIDIA, Dr. Chen, an IEEE Fellow, held senior executive positions at FlexICs, Inc., Taiwan Semiconductor Manufacturing Company, WaferTech LLC, and Cypress Semiconductor Corporation.

In the opening keynote, Dr. Chen reviewed recent market trends driven by the exploding Cloud, mobile and “Internet of Things,” and discussed his perspectives on the challenges of meeting manufacturing and testing needs, while increasing efficiency and reducing overall costs.

“Great talk on overall market trend, challenges and its impact”

Featured Session

The 5G Communication System: A Holistic View

Frank H. P. Fitzek, Technische Universität Dresden

Since 2014, Prof. Frank Fitzek has been leading the Communication Networks at the Technische Universität Dresden, Germany. His current research interests are in the areas of wireless and mobile communication networks, mobile phone programming, network coding and cross layer, as well as energy efficient protocol design and cooperative networking.

In his session, Prof. Fitzek revealed a holistic view of 5G communication systems of the Dresden 5G Lab. In contrast to 2G, 3G, or 4G networks, 5G will not only be characterized by a new air interface, but will also consider changes in the overall network architecture, such as distributed storage, multi-path and more. Prof. Fitzek reviewed 5G use cases, as well as the derived technical challenges and key technologies addressing these challenges.

“Wonderful look into the near future”
“Wow! ”

Track 1: Fine-Pitch Probing Sessions

Direct Probing on Large-Array Fine-Pitch Micro-Bumps of a Wide-I/O Logic-Memory Interface

Ken Smith, Principal Engineer, Cascade Microtech (Co-authored by Erik Jan Marinissen, imec)

In order to obtain acceptable compound stack yields for 2.5D- and 3D-SiCs, there is a need to test the constituting dies before stacking. The non-bottom dies of these stacks have their functional access exclusively through large arrays of fine-pitch micro-bumps, which are too dense for conventional probe

“Great talk on overall market trend, challenges and its impact”
A common approach to obtain pre-bond test access is to equip these dies with dedicated pre-bond probe pads, which comes with drawbacks such as increased silicon area, test application time and reduced interconnect performance. In order to avoid the many drawbacks of dedicated pre-bond probe pads, Ken advocated the usage of advanced probe card technology that allows to directly probe on these micro-bumps, and discussed the technical and economical feasibility of this approach.

**Small-Pad Probing on 40 µm Al/Cu Pads Over Temperature**

Koby Duckworth, Senior Applications Engineer, Cascade Microtech

(Originated by Daniel Ouellette, IBM)

Leading-edge device characterization relies on the precise, repeatable measurement of very small values. The test system contribution to any measured values must either be insignificant when compared to the device measurements, or be highly predictable. In addition, time-to-market pressures drive engineers to test early device prototypes as soon as possible. However, the challenge with early testing is the fact that most fabs currently use copper as their normal interconnect metal. Copper is difficult to contact reliably under the best of circumstances, and when testing occurs at elevated temperatures, concerns about oxidation, as well as contact resistance, have driven most OEMs to cap their copper interconnects and pads with aluminum. This process adds time, risk and variation to devices to be tested. In this session, Koby reviewed the alternatives available with today’s characterization systems for bare copper, multi-temperature testing on small pads using simplified macros for in-test de-embedding and processing monitoring.

**Improving Signal Integrity through Advanced Probe Card Design and Metrology**

John Strom, Technical Fellow, Rudolph Technologies

Jeff Arasmith, Senior Applications Engineer, Cascade Microtech

The market trends for smaller diameter pads, pillars and bumps, and also for higher bandwidth or better signal integrity present challenges to probe card design. Probes with small diameter probe tips provide new capabilities for testing small pad/bump geometries. Short probe tips bring the space transformer closer to the device under test (DUT), but provide challenges to probe card metrology tools. While shorter tips improve signal integrity, the reduced distance from the probe tip to the space transformer challenges the probe tip recognition system in metrology tools. Smaller diameter tips also make visual tip recognition more difficult and they are more sensitive to force and displacement during contact for electrical measurements. When using a monolithic probe core, all the probe tips are overdriven together. This can cause the core to be damaged if it is not fully supported and probe tips are overtraveled individually. Probe card metrology tools face unique challenges to fully characterize individual probe tip positions and electrical properties without damaging the probe card. John and Jeff discussed how to achieve optimum signal integrity when testing emerging device technologies using advanced probe cards and probe card metrology tools.

**Track 2: Sub-THz Probing Sessions**

**On-Wafer Antenna Probes at Sub-THz Frequencies**

Jerry Shiao, Associate Researcher, National Nano Device Laboratories

As sub-THz applications are emerging in both academic and commercial markets to date, Monolithic Microwave Integrated Circuits (MMICs) have become critical RF devices to develop associated products. However, MMIC pads for signal transmission cause great difficulties in on-wafer testing and packaging at such frequencies. Thus, on-chip antennas have been widely suggested to be a better solution at sub-THz signal transmission. To measure these on-chip antennas at the wafer level, NDL has designed antenna probes at 330-500 GHz and 500-750 GHz to receive or transmit signals. These probes can be used in both near- and far-field regions due to their compact sizes. While they precisely cover the antenna beam and minimize surrounding interference, the probes are mounted on general probe stations. NDL has tried several methods to develop new calibration. The on-chip antennas are slot antennas, which can pass modern semiconductor process design rules. Jerry introduced his antenna probe design, measurement setup, calibration method, on-chip slot antennas, simulations and measurement results.

**Development of Compact VNA Extenders to 750 GHz**

Jeffrey Hesler, Virginia Diodes

Virginia Diodes has developed a series of VNA extenders with significantly reduced size that maintain state-of-the-art performance, and are thus well suited for on-wafer probing. For example, the volumes of the extenders from WR-15 (50-75 GHz) thru WR-5.1 (110-170 GHz) have been reduced by 75% while retaining the same dynamic range (120 dB typ.), stability and test port power. In addition, a WM-380 (WR-1.5, 500-750 GHz) extender with reduced size has been developed, enabling 4-port on-wafer measurements up to 750 GHz. Performance and measurements using these extenders were presented in this session.
Techniques to Evaluate RF Test Cell Repeatability and Accuracy

Gavin Fisher, Senior Applications Engineer, Cascade Microtech

Modern device models rely heavily on extractions based on S-parameter measurements. As a part of the Wafer-level Measurement Solutions (WMS) offering from Cascade Microtech and Keysight Technologies, it was necessary to conduct a rigorous study of RF test cell accuracy and repeatability at 26.5, 50, 67 and 110 GHz at ambient and at elevated temperature. In this presentation, Gavin discussed the methods that can be employed using the WinCal XE™ calibration software and comparatively simple coding using Microsoft.Net’s programming environment. Armed with these tools it was possible to evaluate:

- Variation of calibration coefficients from multiple calibrations at single or multiple calibration sites
- Variation of computed open response from single or multiple calibration sites
- Variation of measurement response of independent line standards not used during calibration and of significantly different impedance
- System drift with time
- Standard lifetime

These methods were essential to benchmark system performance, and in one test case, highlighted a system setup issue which otherwise was not immediately apparent from calibration verification alone.

Track 3: Advanced Techniques Sessions

Improvements in On-Wafer MMICs Testing through ATE Systems

Antonio Nanni, Microwave Production and Test Engineer, Selex ES

Selex ES has developed a substantial degree of competitiveness in the design and production of microwave and millimeter-wave systems. This competitiveness is based on high-skill competence related to the fabrication, design and RF testing of power GaAs and GaN MMICs. In particular, the capability to test MMICs at the wafer level through Automatic Test Equipment (ATE) is mandatory to reduce manufacturing costs, time and improve yield. The developed on-wafer ATE allows 100% on-wafer RF screening of millimeter-wave MMICs and HPA-DALNA. The physical implementation of the on-wafer test system is based principally on a semi-automated Alessi REL-6100 station, a non-linear vector analyzer and a Noise Figure Analyzer. The test software is based on LabView and allowing to communicate directly with the chuck controller and all measurement instruments through GPIB commands. The test software is modular, making it easily adaptable to requirements, and it is attached to a linked database for rapid data analysis and chip delivery. Through these features, it is possible to test automatically HPA, DA and LNA up to 26 GHz on the entire wafers. Antonio discussed how the developed ATE system can reduce 90% of the testing time and human errors, and improve accuracy.

Advances in Low-Frequency Noise Measurements

Roberto Tinti, Device Modeling Product Planner, EEsofED, Keysight Technologies

Flicker noise and Random Telegraph Noise (RTN), often collectively known as low-frequency noise, have long been considered critical characteristics of electronic devices. It significantly affects performance of a number of basic building blocks of analog, RF and memory circuits. It is also a key indicator of process and material quality in semiconductor manufacturing. As the semiconductor industry continues to advance new technologies, the need for fast, accurate and repeatable characterization of low-frequency noise has never been greater. Roberto discussed the importance and physical causes of low frequency noise, explained the measurement process, and reviewed various key design considerations that have gone into Keysight’s newest wafer-level flicker noise and RTN measurement system, E4727A, the Advanced Low-Frequency Noise Analyzer. Sample measurement results from wafers of major semiconductor companies were also showcased.
Test Methodology Adaptation for Electromigration Testing of Advanced Back-End-Of-Line CMOS Technologies

Kristof Croes, Team Leader, Electrical and Functional Test and Reliability, imec
Eric Wilcox, Applications Specialist, Cascade Microtech

As electromigration is a key reliability concern for back-end-of-line interconnects, test methodologies are well established, where standards exist for many years already. Electromigration is a current-driven process and today’s test methodologies, thus consist in applying a constant current through the test line at elevated temperatures, while the voltage-drop over the line is monitored over time to electrically monitor void formation. For N10-technology nodes and higher, copper lines are surrounded by thick (>3 nm) and conductive metallic barriers at their bottoms and sidewalls. Such barriers allow for so-called current shunting, where, when voids are big, the current flows through these barriers. A consequence is that voltage-drops over void remain limited, even when high currents are applied. For advanced CMOS technologies below the N10-node, the above mentioned metallic barriers will a) need dramatic scaling or b) be replaced by non-conductive barriers. With such extremely thin semi- or non-conductive barriers, sending a constant current through the test line will induce high voltages over voids. Such high-voltage drops are not happening in real products as chip performance is voltage-limited. Given the above considerations, Kristof and Eric believe revisions of today’s electromigration test methodologies are appropriate, where they want to put forward constant voltage testing as a candidate to replace constant current testing.

High-CURRENT, High-Temperature Measurement Setup

Klaus Kelting, Senior Staff Engineer, Infineon Technologies

A measurement setup covering the temperature range of 0°C up to 500°C is presented. The system is based on a converted Summit™ 12000 probe station. It utilizes nitrogen gas as a protective (anti-oxidation) gas and as a coolant agent. A ceramic chuck prevents unintentional soldering events, as well as accidental oxidation. It also prevents Eddy currents working against current direction of a current pulse. The maximum currents for this setup have not yet been found.

High-Voltage Discrete Device On-Wafer Capacitance Characterization

Mehrdad Baghaie Yazdi, Senior Engineer, Discrete Design Enablement Team, Fairchild Semiconductor

Accurate characterization and modeling of high-voltage discrete devices, such as super junction MOSFETs and IGBTs, are critical for power conversion system-level simulation. Conventional discrete device capacitances, such as the input capacitance CISS, the output capacitance COSS, and the reverse capacitance CRSS for power MOSFETs (CIES, COES, CRES in IGBTs), greatly influence discrete device dynamic circuit performance, in particular the critical dynamic losses, EOFF and EON, and the gate charge characteristics. In particular, CISS (CIES) presents numerous challenges in an on-wafer environment due to the combination of the extracted gate to source (emitter) and gate to drain (collector) capacitances. The work in this presentation advances the state-of-the-art through development of highly accurate high-voltage on-wafer capacitance measurement set-ups and techniques. The measurement set-ups are implemented for Cascade Microtech’s Tesla probe station in combination with the Agilent B1505A analyzer. Results were presented for power MOSFETs and IGBTs ranging from 600 V to 1200 V.
Simplifying Instrumentation and Prober Configuration for On-Wafer Power Device Characterization

Lee Stauffer, Senior Staff Technologist, Keithley Instruments

On-wafer characterization of high-power semiconductor devices involves several different types of measurements: on-state (high-current I-V), off-state (high-voltage I-V), and capacitance-voltage (C-V) at high bias voltages. Unfortunately, each of these measurements involves complex reconfiguration including different instrumentation, cabling, electrical connections and probes. Operator safety cannot be compromised, and the goal of course is valid measurement data. Keithley will discuss ways to simplify the test setup between high-voltage I-V, high-current I-V, and high-voltage C-V power device measurements. Doing so will save time, increase measurement confidence, deliver optimal results, keep the operator safe, and reduce the risk of equipment damage. Specific attention will be paid to high-voltage C-V where optimal measurements can be especially challenging.

Partners and Networking Opportunities

This year’s COMPASS sponsors added value to the conference through showcase of their products and capabilities during networking sessions.

Many of the attendees cited networking with Cascade Microtech’s technical experts and learning from other attendees as the most valuable aspect of the event. Throughout the event, including during sessions, roundtable lunch and evening receptions, attendees were having enthusiastic discussions and actively sharing ideas and knowledge.

The most valuable thing at COMPASS 2014 was…..

“Meeting other users and discussing issues”
“Exchanging facing challenges with other engineers”
“Building up the network”

COMPASS 2014 Sponsors:
Overall, COMPASS 2014 was another great success, showcasing that collaboration is a crucial element for the development of innovative test technologies for tomorrow.

“Great conference! Keep it alive!”

We would like to thank everyone who participated this year:

**Steering Committee**
WaiFai Yee, Microchip
Catherine Savage, Cascade Microtech
Eric Wilms, Cascade Microtech
Junko Nakaya, Cascade Microtech
Laurie Winton, Cascade Microtech

**Technical Committee**
Daniel Bock (chair), Cascade Microtech
Ruben Zowada (chair), Cascade Microtech
James Victory, Fairchild Semiconductor
Jeff Arasmith, Cascade Microtech
Koby Duckworth, Cascade Microtech
Micki Marion, Avago
Richard Campbell, Portland State University

Watch for updates at [www.compass.cascademicrotech.com](http://www.compass.cascademicrotech.com), and if you would like to present at or participate on the committee for COMPASS 2015, please contact us at [compass@cmicro.com](mailto:compass@cmicro.com).

We look forward to COMPASS 2015 and hope to see you next year.